# Integration of High-*k* Oxide on MoS₂ by Using Ozone Pretreatment for High-Performance MoS₂ Top-Gated Transistor with Thickness-Dependent Carrier Scattering Investigation

*Jingli Wang, Songlin Li, Xuming Zou, Johnny Ho, Lei Liao,\* Xiangheng Xiao, Changzhong Jiang, Weida Hu, Jianlu Wang, and Jinchai Li*

In recent years, an extensive amount of studies has been conducted to explore 2D materials such as graphene[1–5] and transition metal dichalcogenides (TMDs)[6–16] for their unique structural features as well as outstanding electrical properties since their first discovery in 2004. Importantly, the atomic thickness makes them the better choices than traditional semiconductors at the device-scaling limit, which is of great importance in circuit integration.[17–21] Graphene has been demonstrated with the ultrahigh carrier mobility as a promising substitute for silicon. However, its lack of bandgap would inevitably yield low device on/off current ratio, limiting its use in switching applications.[2,6] Unlike graphene, MoS₂, as a representative of TMDs, has an intrinsic bandgap ranging from 1.2 to 1.8 eV depending on the flake thickness.[22] This large band gap can not only enable the relatively high device on/off ratio but also enhance its ability to screen external potential fluctuations, both of which make it a superior channel material for logic devices.[6–16]

At the same time, in order to address and operate transistors individually in integrated circuits, it is necessary to fabricate local top gates for all transistors. Integration of MoS₂ field effect transistors (FETs) requires the ability to grow or deposit high-quality, ultrathin dielectric insulators on MoS₂. However, it is extremely difficult to deposit atomically thin dielectrics onto the dangling bond-free MoS₂ surface.[23] Direct deposition will result in large isolated grain and cannot acquire thin dielectric.[24] Lately, we have also demonstrated that the appropriate interface engineering, such as employing an $Y_2O_3$ buffer layer, can greatly improve the dielectric/channel interface quality and the consequent electrical performance of top-gated MoS₂ transistors.[23] However, the $Y_2O_3$ buffer layer will greatly decrease the capacitance of the top gate dielectric, which goes against the purpose of applying high-*k* materials. Furthermore, the buffer layer can only be deposited on top of the devices, which makes it difficult to fabricate devices with complex structure. Therefore, developing a method for direct deposition of high-*k* material without buffer layer is of great importance.

On the other hand, due to the lattice phonon vibration, the theoretical limit of carrier mobility in single-layer MoS₂ is estimated to be 410 cm² V⁻¹ s⁻¹ at room temperature, which is comparable to that of silicon.[8,13,25] Nevertheless, all previously reported mobility values of MoS₂ are much lower than the lattice phonon limit.[10] Even after healing the intrinsic sulfur vacancies in the monolayer MoS₂, the highest mobility value is still only up to 81 cm² V⁻¹ s⁻¹ at room temperature, significantly lower than the theoretical limit.[26] All these explicitly indicate that the device performance of current MoS₂ transistors is greatly restricted by extrinsic carrier scattering. Previous report indicated that depositing high-*k* material can improve the mobility of MoS₂ devices, but subsequent work point out that the mobility promotion may be due to gate coupling.[16] Depositing high-*k* material can screen the charge impurities and get rid of absorbed $H_2O$ and $O_2$, but new charge impurities and surface phonon may be introduced as new scattering centers, which may decrease the carrier mobility.[27] The fabricating condition of dielectric layers is expected to strongly affect the carrier transport in ultrathin MoS₂ channels since the extrinsic carrier scattering at the dielectric/channel interfaces is ineluctable. Researches

Dr. J. Wang, Dr. X. Zou, Prof. L. Liao, Prof. X. Xiao, Prof. C. Jiang, Prof. J. Li
Department of Physics and Key Laboratory of Artificial Micro- and Nano-Structures of Ministry of Education
Wuhan University
Wuhan 430072, China
E-mail: liaolei@whu.edu.cn

Prof. S. Li
WPI Center for Materials Nanoarchitechtonics and International Center for Young Scientist
National Institute for Materials Science
Tsukuba, Ibaraki 305-0044, Japan

Prof. J. Ho
Department of Physics and Materials Science
City University of Hong Kong
Tat Chee Avenue, Kowloon
Hong Kong SAR 999077, China

Prof. W. Hu, Prof. J. Wang
National Laboratory for Infrared Physics
Shanghai Institute of Technical Physics
Chinese Academy of Sciences
Shanghai 200083, China

on the influence brought by depositing high-$k$ materials used to be limited in the bottom-gated mobility. However, the top-gated and bottom-gated mobility might be different because the carrier distribution and scattering are different. Till now, little has been done regarding the influence of interface quality of top-gated dielectrics on the performance of transistors based on atomically thin 2D dichalcogenides. In this regard, it is extremely important to perform a systematic study to investigate and control the influence of high-$k$ material on the top-gated mobility of $MoS_2$.

In this work, we use a novel and facile approach to deposit high-$k$ dielectrics (such as $HfO_2$) to fabricate high-performance top-gated transistors and perform a detailed statistical study for the first time to investigate the influence on top-gated mobility brought by the deposition of $HfO_2$. Devices with 10 nm thick $HfO_2$ gate dielectric are fabricated and the highest field effect mobility is as high as 46 $cm^2$ $V^{-1}$ $s^{-1}$. Impressive leakage current about 0.2 pA $mm^{-2}$ at 6.5 MV $cm^{-1}$ is acquired when the gate dielectric is reduced to 6 nm and this is the thinnest gate dielectric for $MoS_2$ transistors. Due to the thickness-dependent top-gated mobility decrease, it can be inferred that choosing appropriate $MoS_2$ thickness can effectively control the influence brought by deposition of $HfO_2$. For monolayer ones, top-gated mobility is greatly suppressed while multilayer ones show better tolerance. $MoS_2$ transistors with 2–3 layers show relatively high tolerance in the low trap density region. Considering the negative shift of threshold voltage with the increase of flake thickness, 2–3 layers are more suitable for logic devices and thicker ones are more suitable for devices with higher output current. Utilizing the optimized channel length and strong gate control, high drain current density of 612 μA $μm^{-1}$ is achieved in the multilayer $MoS_2$ with a channel length of 250 nm, in which, to the best of our knowledge, is the highest room-temperature output current in all $MoS_2$ transistors reported till now.[23,28]

Here, the $MoS_2$ flake is mechanically exfoliated onto the $SiO_2$/Si (255 nm thick thermal oxide) substrate by the scotch tape method.[1] The thickness of these $MoS_2$ flakes is evaluated by optical microscopy and Raman spectroscopy. FETs with 1.5 μm channel length are fabricated using e-beam lithography and 15/50 nm thick Ni/Au is used as the contact electrode to form an ohmic contact. In order to enable direct deposition of top-gated dielectrics, a preliminary UV–O treatment is employed to functionalize $MoS_2$ surfaces. Then, a direct deposition of 10 nm thick $HfO_2$ is performed under a relatively low temperature of 95 °C as the top-gated dielectric and this low deposition temperature are purposely employed to avoid thermal damage to the channel, which gives rise to a dielectric constant of $HfO_2$ being 11. After that, 15/50 nm thick Cr/Au is employed as the top-gated electrode to operate the FET. The device schematic and scanning electron microscope (SEM) image of the representative $MoS_2$ FET are given in **Figure 1**a,b.

Atomic force microscopy (AFM) is used to identify the thickness of $MoS_2$ and quality (i.e., morphology) of the deposited $HfO_2$. As depicted in Figure 1c, the as-exfoliated $MoS_2$ flake is smooth with the thickness ranging from 0.7 nm to 2.1 nm (Figure S1, Supporting Information), consisting of monolayer to trilayer of $MoS_2$. Then, the corresponding AFM image after the deposition of $HfO_2$ is given in Figure 1d, which demonstrates the good uniformity of the deposited dielectric film with almost no pinhole (image of as-exfoliated, UV–O treated and dielectric deposited $MoS_2$ flakes with different thickness is given in Figure S2, Supporting Information). The X-ray photoelectron spectroscopy (XPS) is applied to see whether the $MoS_2$ flake is oxidized during the UV–O treatment (Figure S3, Supporting Information).
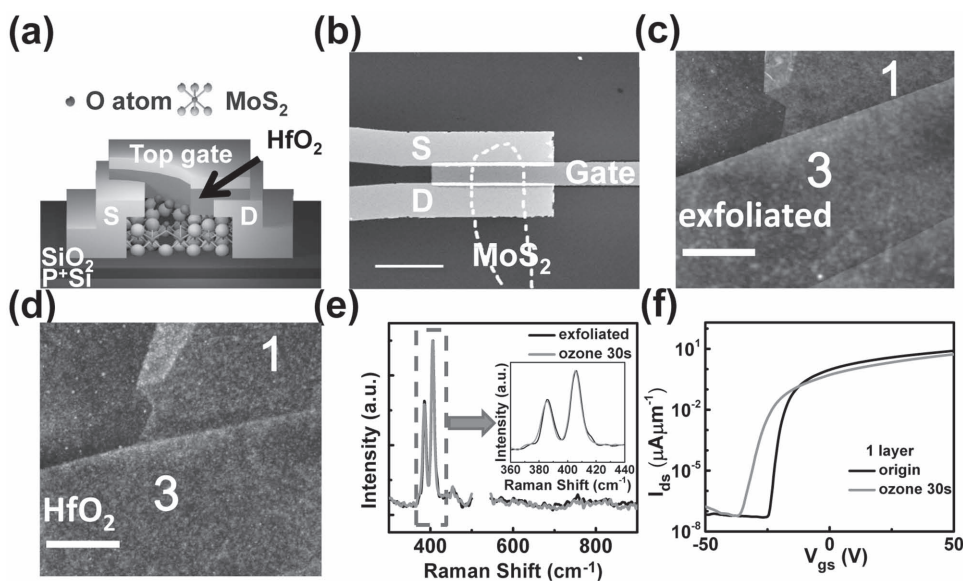


**Figure 1.** a) Device schematic of the top-gated $MoS_2$ FET. b) SEM image of the representative top-gated transistor; the scale bar is 5 μm. c) AFM image of the as-exfoliated $MoS_2$ flake; the scale bar is 500 nm. d) AFM image of the same $MoS_2$ flake after 10 nm thick $HfO_2$ is deposited. e) Raman spectra of the as-exfoliated and the ozone treated $MoS_2$ flake, the peak of the $SiO_2$/Si substrate at 520.7 $cm^{-1}$ is erased. No $MoO_3$ peak at 820 $cm^{-1}$ is seen and the small negative shift shows slight n-type doping. f) Transfer characteristics of the origin and UV–O treated $MoS_2$ devices. Both the mobility and the drain current have been decreased slightly after the treatment.

The Mo 3d, S 2s, and S 2p peak show no shift after the UV–O treatment and there is no additional peak observed. This is different from previous report with new double peak observed at 164.8 eV after 5 min treatment.[29] This may be explained by the 30 s rapid treatment time employed and the $N_2$ protect gas. Previous work shows that the peak for S—O bond increase with process time and it is small even with 5 min UV–O treatment time. It can be surmised that S—O bond created during the rapid 30 s process is below detection. The $N_2$ in the UV–O system plays as protective gas, it protects the $MoS_2$ from too much oxidation and mobility decline.[9] To further assess the potential doping effect and possible lattice damage of the channel during the UV–O treatment, Raman spectra are collected for samples before and after the treatment.[30] The Raman spectra of exfoliated and UV–O treated $MoS_2$ are illustrated in Figure 1e. For the untreated sample, the in-plane peak is located at 384 $cm^{-1}$ and the out-of-plane peak is located at 402 $cm^{-1}$. The UV–O treated $MoS_2$ shows a small negative shift with 1.1 $cm^{-1}$, indicating slight n-type doping. This may attribute to the $N_2$ protect gas. Being exposed to $N_2$ gas with ultraviolet light can result in n-type doping for $MoS_2$.[9] Notably, the absence of the $MoO_3$ Raman peak at 820 $cm^{-1}$ after the treatment indicates no Mo—O bond formation during the UV–O process, which suggests that the gentle UV–O treatment does not introduce any noticeable lattice damage or bond disorder into the $MoS_2$ flake, in agreement with the XPS result and previous reports (Raman spectra image of $MoS_2$ with different thickness is given in Figure S4, Supporting Information).[29,30] Since the dielectric is now deposited with the highly improved coverage onto $MoS_2$ (Figure 1d), it can be inferred that a small number of dangling bonds has been introduced onto $MoS_2$ during the UV–O treatment, otherwise there would not be any effective nucleation centers for the observed uniform dielectric growth. Also, the transfer characteristics of the pristine and UV–O treated bottom-gated transistors are given in Figure 1f. The small negative shift of

the threshold voltage indicates slight n-type doping, which coincides with the negative Raman shift. Both the drain current and mobility show a slight decrease in the UV–O treated sample, further confirming the presence of additional carrier scattering centers introduced by the UV–O treatment.

To investigate the effect of different flake thickness on the transport behavior of $MoS_2$ FETs, device channels with varied thickness of 1–4 layers of $MoS_2$ are fabricated. **Figure 2**a shows the typical transfer characteristics of top-gated $MoS_2$ transistors with different channel thicknesses. From monolayer to quadlayer, the threshold voltage reveals some variation but still exhibits the trend of negative shift. The field effect mobility is then calculated as

$$\mu = \frac{L}{W} \cdot \frac{g_m}{C_i V_{ds}} \tag{1}$$

where $L$ and $W$ represent the device channel length and width, respectively, $C_i$ is the capacitance of 970 nF $cm^{-2}$, $V_{ds}$ is the source–drain voltage and $g_m$ signifies the transconductance of the linear region. As depicted in Figure 2b, the transistor with four layers of $MoS_2$ channel gives the largest field effect mobility of 46 $cm^2$ $V^{-1}$ $s^{-1}$. As compared with others, transistors with 1–3 layers of $MoS_2$ have relatively low mobility values of 16, 22, and 39 $cm^2$ $V^{-1}$ $s^{-1}$, accordingly. As well, Figure 2c–f displays the corresponding output characteristics of the same devices studied in Figure 2a. These output curves in the linear region exhibit relatively good linear relationship at low $V_{ds}$, indicating ohmic contact properties and good transistor characteristics.

At the same time, **Figure 3**a,b gives the statistical analysis of field effect mobility calculated for the bottom- and top-gated devices with different channel thicknesses. For bottom-gated transistors, the average mobility, $u_{bg}$, increases from 29, 34, and 43 to 51 $cm^2$ $V^{-1}$ $s^{-1}$, when the flake goes from the monolayer to quad layers of $MoS_2$, respectively. After the deposition of 10 nm thick $HfO_2$ and fabrication
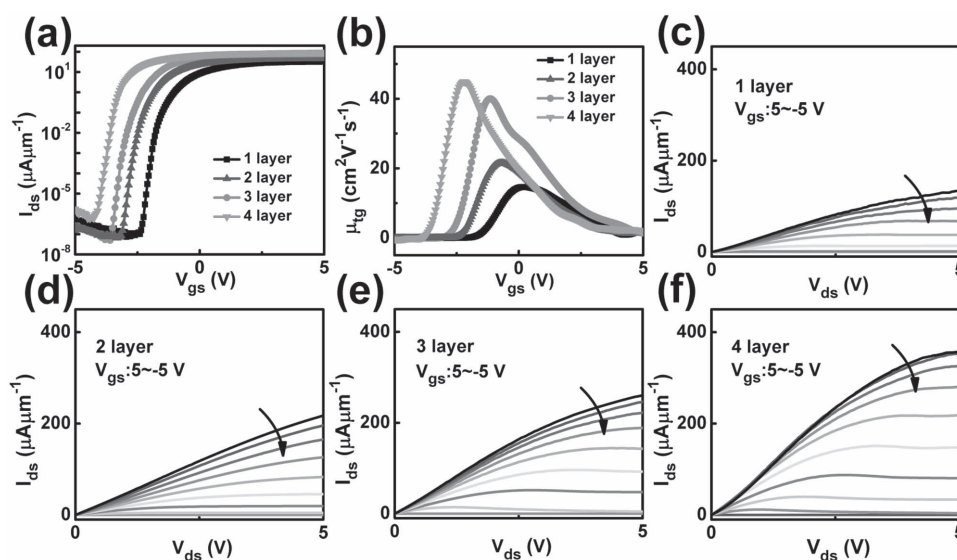


**Figure 2.** a) Transfer curves of the $MoS_2$ FETs with different channel thickness ranging from 1 to 4 layers, $V_{ds}$ = 1 V; the channel length is 1.5 µm. b) The calculated mobility of the devices is given in Figure 2a. c–f) The output curves of the devices given in Figure 2a, all show good linear relationship in the low $V_{ds}$ region.
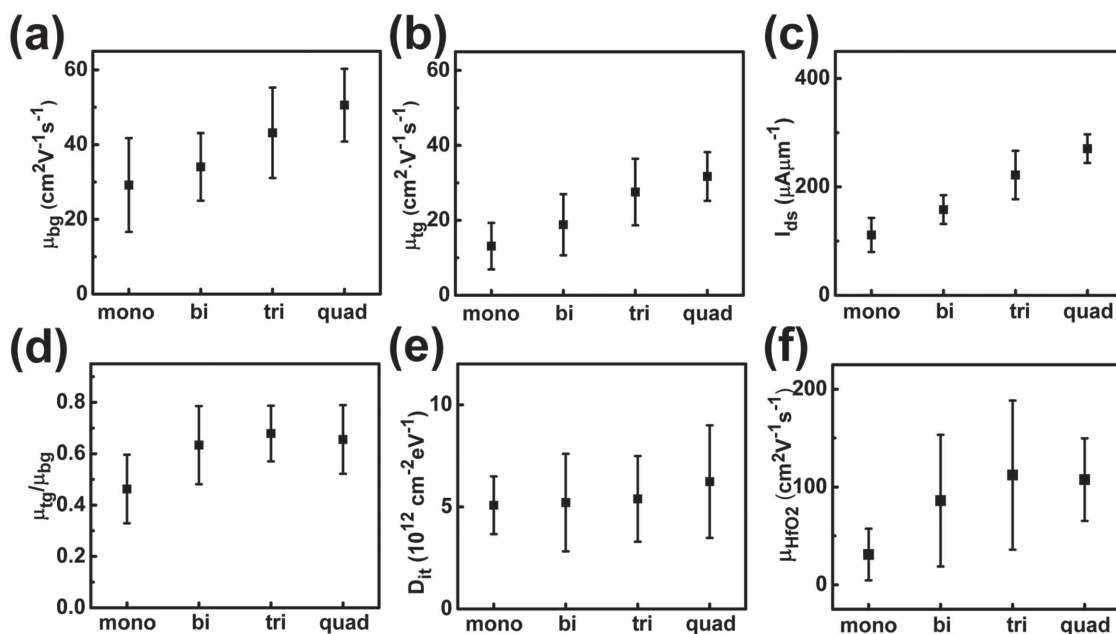
**Figure 3.** Statistical result of the MoS$_2$ FET characteristics with different channel thicknesses and the error bar represent device-to-device variation. The statistical data include a) bottom-gated mobility, b) top-gated mobility, c) saturated drain current density, d) ratio between top- and bottom-gated mobility, e) trap density, and f) the limited mobility.

of top-gated electrode, the average top-gated field effect mobility, $u_{tg}$, decreases to 13, 19, 28, and 32 cm$^2$ V$^{-1}$ s$^{-1}$, accordingly. Besides, the saturation current also shows the similar uptrend from 111 μA μm$^{-1}$ to 270 μA μm$^{-1}$ as illustrated in Figure 3c.

Next, a detailed comparison of device performance is made between the top- and bottom-gated structures in order to assess the influence of UV–O treatment and top-gated dielectric deposition on the electrical transport properties of MoS$_2$ devices. Due to the two-probe method, the contact resistance ($R_c$) is included in the total device resistance ($R_{total}$). To get rid of the influence of contact resistance, the contact resistance percentage of the total resistance is given by transfer length method in Figure S5 (Supporting Information). The trend of $R_c/R_{total}$ with increased MoS$_2$ thickness and $V_{gs}$ is similar to the previous report.[21] Due to the average $R_c/R_{total}$ with various $V_g$, it can be inferred that both the bottom-gated and top-gated mobility are partly affected by the contact resistance. To rule out the device variation, we employ the ratio of $\mu_{tg}/\mu_{bg}$ to evaluate the influence of the UV–O treatment and dielectric deposition. The average $\mu_{tg}/\mu_{bg}$ ratio along with their standard deviation for different flake thickness is given in Figure 3d. As compared with Figure 1f, which shows the mobility degradation by the UV–O treatment, the more drastic mobility decrease with a $\mu_{tg}/\mu_{bg}$ ratio of 0.45 is observed in the top-gated monolayer samples. The contact resistance does show different $R_c/R_{total}$ with different $V_{gs}$, but the ratio and changes are rather small compared with the large mobility decrease. By long time annealing and vacuuming, we can dislodge the charge impurities and obtain high bottom-gated mobility. The UV–O treatment and ALD deposition process will introduce new impurities and remote phonon scattering, which will decrease the mobility.[27] Although the

high-$k$ material can screen the Coulomb reaction, it may not compensate the newly introduced Coulomb reaction and remote phonon scattering. Again, the $\mu_{tg}/\mu_{bg}$ ratio also demonstrates the strong thickness dependence, with the ratio increasing from 0.45 to 0.65 as the thickness increases from 1 to 4 layers. By carefully choosing appropriate channel thickness, we can control the influence brought by the deposition of HfO$_2$.

To further quantify the interface quality of top-gated samples, we adopt interface trap density, $D_{it}$, as the criterion that can be calculated as

$$D_{it} = \frac{C_i}{q}\left(\frac{q \cdot SS}{kT \ln 10} - 1\right) \qquad (2)$$

where $C_i$ represents the capacitance per unit area, $q$ designates the electron charge, SS is the subthreshold slope, and $T$ signifies the test temperature.[23,31] It is found that the average layer-dependent $D_{it}$ of these top-gated transistors are 5.1, 5.2, 5.4, and 6.2 × 10$^{12}$ cm$^{-2}$ eV$^{-1}$, respectively, for 1 to 4 layers of MoS$_2$ (Figure 3e), illustrating a reasonably good interface quality between MoS$_2$ and HfO$_2$. A slightly higher trap density is observed in the multilayer MoS$_2$ devices, which can be explained owing to the quantum capacitance, $C_q$, of the electron charge.[31–35] Specifically, the series connection of $C_q$ and oxide capacitance $C_{ox}$ would yield the total device capacitance, $C_g^{-1} = C_{ox}^{-1} + C_q^{-1}$. This way, $C_g$ of the top-gated devices and the calculated $D_{it}$ will be modulated accordingly with different $C_q$. On the other hand, as $C_q$ is directly related to the density of states (DOS), the trend of DOS can be deduced from the variation tendency of the calculated $D_{it}$.[33] Therefore, from the uptrend of $D_{it}$, we can estimate that the DOS is expected to increase slightly with increased flake thickness. All these are perfectly consistent to

the DOS variation induced by the interaction between layers of the multilayer MoS$_2$ flake, which prove the validity of the calculated $D_{it}$.

In contrast, the mobility of free carriers can also be expressed as $\mu_e = e\langle\tau\rangle/m_e$ where $m_e$ is the effective mass of electrons and $\langle\tau\rangle = \dfrac{\int_0^\infty \tau(E)\frac{\partial f_0}{\partial E} E^{\frac{3}{2}} dE}{\int_0^\infty \tau(E)\frac{\partial f_0}{\partial E} E^{\frac{3}{2}} dE}$.[36] The total relaxation time can be presented as $\dfrac{1}{\tau} = \sum_i \dfrac{1}{\tau_i}$ where $\tau_i$ is the corresponding relaxation time for different scattering mechanism. Due to the linear relationship of $\mu_e$ and $\langle\tau\rangle$, the free carrier mobility can be as well expressed as $\dfrac{1}{\mu} = \sum_i \dfrac{1}{\mu_i}$ where $\mu_i$ is the mobility limited by different kinds of scattering events. In any case, charge impurities and short-range defects are believed to be the main scattering mechanism in the bottom-gated devices.[26] However, the additional surface optical phonon and dangling bonds introduced by the high-k dielectric deposition are found to be strong scattering sources in the top-gated devices, in which this scattering effect can be estimated by comparing the mobility values between the bottom- and top-gated structures. For the bottom-gated structure, the bottom-gated mobility can be expressed as $\dfrac{1}{\mu b} = \sum_i \dfrac{1}{\mu_i}$. For the top-gated device, the additional scattering would contribute to one more term of $\mu_{HfO2}$ in the mobility formula $\dfrac{1}{\mu t} = \sum_i \dfrac{1}{\mu_i} + \dfrac{1}{\mu_{HfO_2}}$.[25,26] As a result, the additional scattering from HfO$_2$ dielectric and the corresponding limited mobility ($\mu_{HfO2}$) can be calculated by $\dfrac{1}{\mu_{HfO_2}} = \dfrac{1}{\mu t} - \dfrac{1}{\mu_b}$. Likewise, Figure 3f illustrates the average $\mu_{HfO2}$ calculated from the bottom- and top-gated mobility for different thickness of MoS$_2$. Based on a statistics of more than 20 devices for each channel thickness, the average $\mu_{HfO2}$ for monolayer MoS$_2$ is about 31 cm$^2$ V$^{-1}$ s$^{-1}$ while for bilayer, trilayer, and quadlayer MoS$_2$, the $\mu_{HfO2}$ are 86, 112, and 107 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. It is clear that the average $\mu_{HfO2}$ increases with the channel thickness, indicating the severest limitation to monolayer MoS$_2$ FETs.

In order to further understand the relationship between the dielectric/channel interface quality and electronic transport properties of MoS$_2$ devices, **Figure 4** plots the calculated $\mu_{HfO2}$ against $D_{it}$ and 20 devices are studied for each channel thickness. For all channel thicknesses, the $\mu_{HfO2}$ exhibits a downward trend, in which the mobility enhances with the reducing trap density $D_{it}$. For devices showing the highest $\mu_{HfO2}$ in each thickness, the trap density values are found as 1.4, 2.7, 3.3, and 2.5 × 10$^{12}$ cm$^{-2}$ eV$^{-1}$, accordingly. Nearly each of them represents the best interface quality in the corresponding thickness regime. Among all, the highest $\mu_{HfO2}$ is only 96 cm$^2$ V$^{-1}$ s$^{-1}$ for the best monolayer MoS$_2$ device, which is relatively low as compared with other thickness regime (i.e. 241, 281, and 185 cm$^2$ V$^{-1}$ s$^{-1}$ for the 2–4 layer devices, respectively). This low $\mu_{HfO2}$ of monolayer devices reflects its
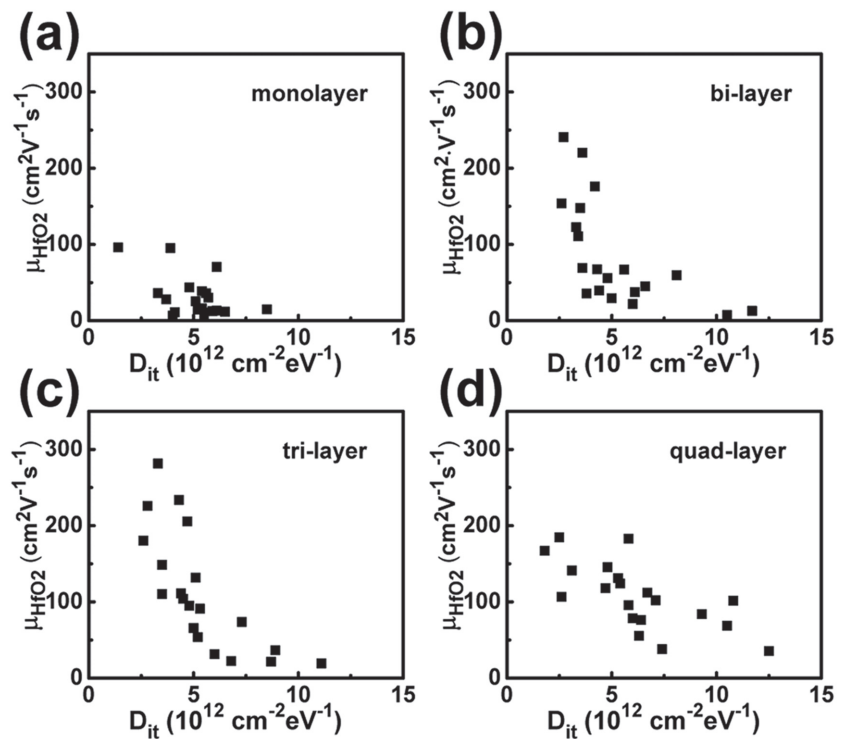


**Figure 4.** The limited mobility against the trap density for MoS$_2$ channel thickness ranging from a) monolayer to d) quadlayer. The HfO$_2$-limited mobility is calculated from top- and bottom-gated mobility.

weak resistibility to the carrier scattering introduced by the top-gated HfO$_2$ dielectric deposition. On the contrary, the $\mu_{HfO2}$ are generally above 100 cm$^{-2}$ V$^{-1}$ s$^{-1}$ for multilayer ones when $D_{it}$ are below 5 × 10$^{12}$ cm$^{-2}$ eV$^{-1}$, affirming their insusceptibility to the carrier scattering sources. Since the introduction of interface traps is inevitable in the top-gated fabrication, it is inferred that multilayer channels are more suitable for fabricating high-performance top-gated MoS$_2$ devices.

The distinctive abilities of scattering susceptibility in different thickness regime can be simply understood according to the theory of carrier distribution and related interaction distance between the interfacial scattering centers and channel carriers.[37] As shown in **Figure 5**a, when the top gate is biased, the carriers are confined close to the HfO$_2$ dielectric and behave as a 2D electron gas.[37] This way, the scattering interaction distance has become larger in the multilayer channel than the monolayer channel, resulting in the lower scattering potential in the multilayer device. Combining with the knowledge of relationship among channel thickness, interface quality, and carrier transport properties of MoS$_2$ devices, we then fabricate the optimized high-performance multilayer MoS$_2$ transistors. Here, by reducing the channel length down to 250 nm, a high output current density of 612 μA μm$^{-1}$ is achieved at $V_{gs}$ = 3 V as depicted in Figure 5b, in which, to the best of our knowledge, is the highest room temperature current density achieved in MoS$_2$ devices reported to date. Moreover, we fabricate a device with 6 nm thick HfO$_2$ top-gated dielectric, which is the thinnest top-gated dielectric for MoS$_2$ transistor to our knowledge. As shown in Figure 5c, the device shows ideal SS of 75 mV dec$^{-1}$ and can be well cut off at $V_{gs}$ = −3 V. The
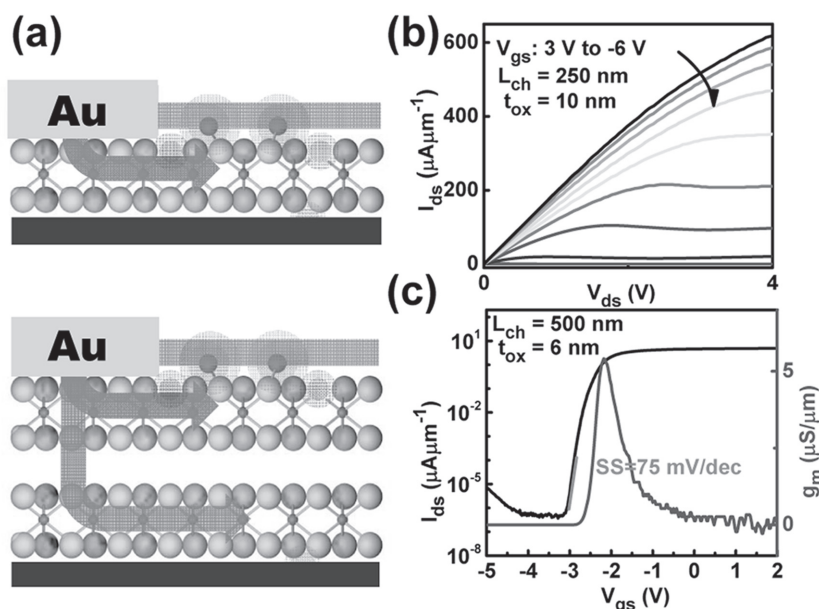
**Figure 5.** a) Charge transport and carrier scattering in monolayer and bilayer MoS$_2$ FETs. The red dots located at the interface represent the external scattering source and the gray dot at the MoS$_2$ body represents the intrinsic charge scattering center and the length of the arrow represents the carrier mobility. b) Output curve of a multilayer MoS$_2$ FET with the channel length of 250 nm. c) Transfer curve of a top-gated device with 6 nm gate dielectric.

impressive leakage current is about 0.2 pA mm$^{-2}$ at 6.5 MV cm$^{-1}$ (Figure S6, Supporting Information), much better than previous work of 2 pA mm$^{-2}$ at 2 MV cm$^{-1}$.[6,31]

In summary, a soft UV–O method is developed to fabricate buffer layer free top-gated MoS$_2$ devices. It is found that the device performance of both monolayer and multilayer MoS$_2$ transistors is strongly influenced by the carrier scattering introduced by the deposition of HfO$_2$ dielectric. By choosing appropriate thickness of MoS$_2$ flake, the influence can be well controlled. Based on the observed relationship between the interface trap density and mobility, it can be inferred that the multilayer MoS$_2$ is more suitable for fabricating high performance top-gated transistors. Due to the negative shift of the threshold voltage with thickness, and the small limitation in the low trap density region, 2–3 layers MoS$_2$ is more suitable for logic devices. For monolayer ones, more work is needed to fabricate high performance top-gated devices, such as reducing the contact resistance and find better way to reduce the scattering. The buffer layer free fabrication process and thickness dependent tolerance for scattering brought by the top gate dielectric deposition will provide a significant insight to 2D devices and guide the roadmap for future development of nanoelectronics.

## Experimental Section

*Materials*: Monolayer MoS$_2$ was prepared by mechanical exfoliation from bulk MoS$_2$ crystal (purchased from SPI supplies). The number of layers in these MoS$_2$ nanosheets was distinguished by Raman spectroscopy and the inspection under optical microscope.

*Device Fabrication*: The source/drain electrodes were deposited through e-beam lithography and lift-off processes. PMMA was used as the resist layers and after the development of the pattern, electrode was deposited by thermal deposition. After the deposition, we used acetone to lift-off the patterns. 30 s UV–O treatment is employed with 253.7 nm and 184.9 nm wavelength. Gate dielectric was grown with KE-MICRO TALD-200A under a low temperature of 95 °C.

*AFM Characterization*: AFM imaging was performed by Bruker Multimode 8 with Scan Assist-Air probe under peak force mode in the ambient condition.

*Electrical Characterization*: Dielectric constant of the HfO$_2$ was obtained by measuring the capacitances with two different thicknesses of dielectric on Si substrate. The capacitance was obtained via Keithley 4200-SCS and the thickness was obtained by AFM characterization. Output and transfer curves were obtained using Agilent 4155C semiconductor parameter analyzer in the vacuum condition at room temperature. Bottom-gated devices were annealed under 220 °C in vacuum with Lakeshore TTPX probe station for 1.5 h and kept in vacuum for over 6 h without exposure to air before test.

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