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Formation and Characterization of $Ni_xInAs/InAs$ Nanowire Heterostructures by Solid Source Reaction

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ABSTRACT

The formation of crystalline Ni_xInAs and $Ni_xInAs/InAs/Ni_xInAs$ heterostructure nanowires by the solid source reaction of InAs nanowires with Ni is reported for the first time. The fundamental kinetics of the Ni/InAs alloying reaction is explored, with the Ni diffusion reported as the rate determining step. The diffusivity of Ni is independent of the nanowire diameter, with an extracted diffusion activation energy of ~1 eV/atom. The metallic Ni_xInAs exhibits a modest resistivity of ~167 $\mu\Omega\cdot$cm for diameters >30 nm, with the resistivity increasing as the nanowire diameter is further reduced due to the enhanced surface scattering. The alloying reaction readily enables the fabrication of $Ni_xInAs/InAs/Ni_xInAs$ heterostructure nanowire transistors for which the length of the InAs segment (i.e., channel length) is controllably reduced through subsequent thermal annealing steps, therefore enabling a systematic study of electrical properties as a function of channel length. From the electrical transport studies, an electron mean free path on the order of a few hundred nm is observed for InAs NWs with a unit length normalized, ON-state resistance of ~7.5 kΩ/μm. This approach presents a route toward the fabrication for high performance InAs nanowire transistors with ohmic nanoscale contacts and low parasitic capacitances and resistances.

One-dimensional nanowires (NWs) have been the focus of intensive research efforts and have been proposed as the building blocks for various technological applications due to their unique physical and chemical behaviors.[1] Specifically, the miniaturized dimensions of NWs provide improved electrostatics for nanoscale transistors, and their ability to be readily assembled or printed on virtually any foreign substrate, including plastic and paper, presents a unique route toward high performance printable macroelectronics.[2] One of the major challenges associated with nanowire devices, and all nanoscale devices in general, is the development of nanoscale and ohmic source/drain (S/D) contacts.[3] Nanoscale dimensions for the contacts are needed to reduce the parasitic capacitances and minimize the drain induced barrier lowering effects while low contact resistivity with ohmic interfaces are desired for reduced parasitic resistances. To address this challenge, recently, Y. Hu, et al., demonstrated sub-100 nm FETs based on $NiGe_xSi_y$-Ge/Si-$NiGe_xSi_y$ nanowire heterostructures in which $NiGe_xSi_y$ was utilized as the nanoscale metal contact to the Si channel.[4] The fabricated transistors display superb electrical properties with minimal short channel effects. Additionally, silicide and germanide contacts are known to exhibit higher chemical stability and lower junction resistance as compared to elemental metal contacts (i.e., pure Ni), which presents another advantage for the alloyed contacts. While silicides and germanides have been well examined and characterized by researchers for both bulk and nanowire structures,[5] to date, metal/InAs alloys have been poorly explored with only limited information available in the literature.[6] Recently, there has been major interest in the use of InAs as the channel material for high performance transistors, as it offers high electron mobility (~10000 cm^2/Vs), and InAs n-FETs, in both thin film and nanowire channel configurations, have already been demonstrated to

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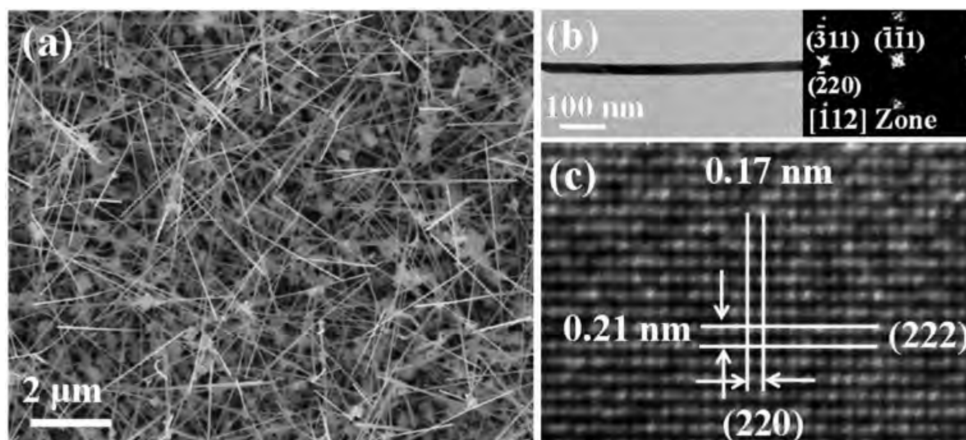

Figure 1. Ni-catalyzed InAs NWs grown on Si/SiO_2 substrates. (a) SEM image of InAs NWs on the growth substrate. (b) TEM image of a representative InAs NW. The corresponding diffraction pattern is shown in the inset, indicating the growth direction of [110]. (c) High resolution TEM image taken from the NW in (b), showing the single crystal feature for which two planes, (222) and (220), are indexed.

outperform conventional Si MOSFETs.[7] Therefore, developing and characterizing metal/InAs alloys with low resistivity and abrupt interfaces as the contact material to InAs is of major interest. Here, we report the formation and materials properties of Ni_xInAs/InAs/Ni_xInAs heterojunction and Ni_xInAs NWs by using a simple solid source reaction of Ni with InAs NWs at annealing temperatures of 220−300 °C in different ambient conditions. The diffusion kinetics of Ni atoms inside InAs NWs and the electrical properties of the fabricated devices with ohmic Ni_xInAs contacts are investigated in detail.

InAs NWs used in this work were synthesized on Si/SiO_2 substrates via the vapor−liquid−solid/vapor−solid−solid process by using Ni nanoparticle seeds as previously reported.[7e] The diameter of the grown InAs NWs is 20−40 nm with length ∼10 μm (Figure 1a). NWs are single crystalline as observed by transmission electron microscopy (TEM) (Figure 1b,c). The grown NWs were drop casted on a Si/SiO_2 (50 nm, thermally grown) substrate followed by the photolithography patterning of S/D electrodes, 5 s 0.5% HF dip, thermal evaporation of Ni (∼50 nm thick), and lift-off. InAs NW devices were then thermally annealed at 220−300 °C for 5−120 min in H_2, N_2, and NH_3 ambient at 40 torr pressure. During the annealing process, Ni atoms diffuse into InAs NWs to form Ni_xInAs (Figure 2a,b). The formation of Ni_xInAs/InAs junctions were observed by optical and scanning electron microscopy (SEM) as the two materials exhibit distinct contrast (Figure 2c).

To examine and characterize the crystalline structure and interface abruptness of the InAs/Ni_xInAs heterojunctions, TEM analysis was utilized. For the TEM sample preparation, InAs NWs were drop-cast on a Si_3N_4 membrane (50 nm thick) grid. Ni pads (∼40 nm thick) were then patterned on the membrane by thermal evaporation through a shadow mask. Subsequently, the sample was annealed at 300 °C for 30 min to form InAs/Ni_xInAs heterojunctions. The atomically abrupt junctions are clearly resolved under TEM, as shown and indicated by the dotted line in Figure 2d. Ni_xInAs is single crystalline. By analyzing the diffraction pattern converted by fast-Fourier transform, the ternary phase is

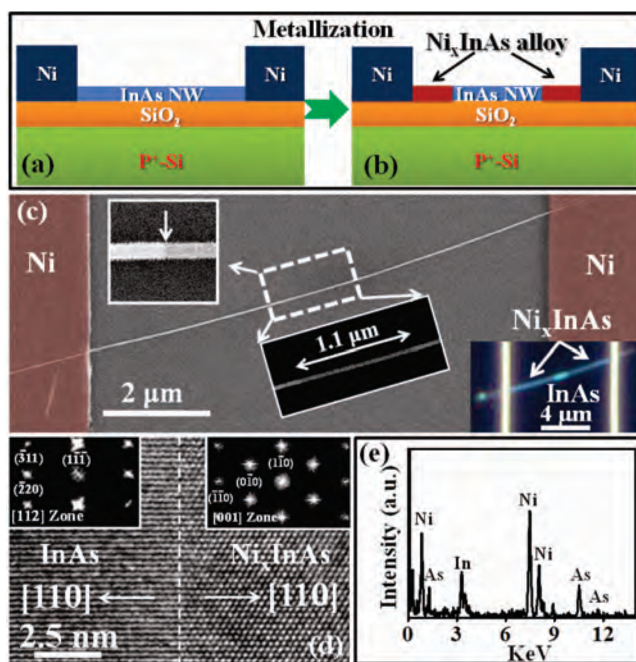

Figure 2. Ni_xInAs/InAs/Ni_xInAs NW heterojunctions. Schematic of the long channel InAs devices with Ni S/D electrodes (a) before and (b) after the thermal annealing process. (c) The corresponding SEM image after the thermal diffusion of Ni. The center inset shows the Ni_xInAs/InAs/Ni_xInAs heterojunction. The high magnification SEM image in the upper inset shows the sharp interface. The bottom inset shows the dark-field optical microscopy image of the same NW device. The bright NW segment in the middle of the device corresponds to InAs, which is connected to Ni_xInAs NW segments at the two ends. (d) High resolution TEM of a InAs/Ni_xInAs heterojunction, showing the atomically abrupt interface. The insets are the corresponding diffraction patterns extracted by Fast-Fourier Transform, indicating the epitaxial relationship of ($\bar{2}$20)InAs//($\bar{1}\bar{1}$0)Ni_xInAs with[112]InAs//[001]Ni_xInAs. (e) Energy dispersive X-ray spectroscopy of Ni_xInAs NW.

identified as Ni_3InAs, which is also roughly consistent with the EDS analysis from which a Ni:In:As atomic ratio of 58:22:20 is obtained (Figure 2e).

To shed light on the metallization mechanism, we explored the reaction kinetics of the Ni/InAs system. First, we explored

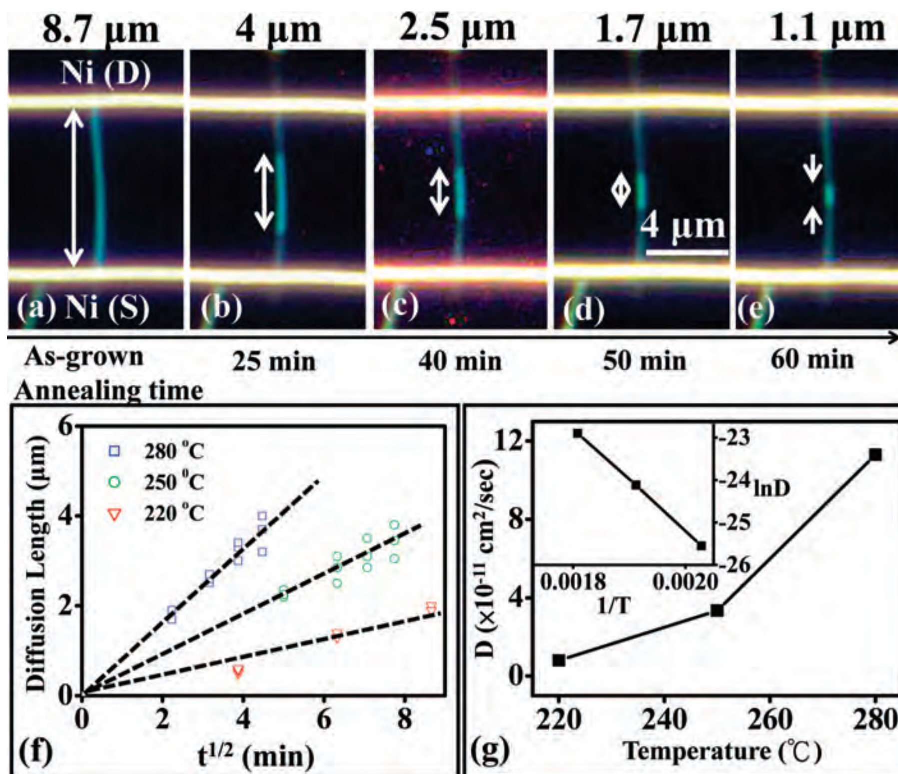

Figure 3. Kinetics studies of Ni_xInAs formation by a solid source reaction. (a−e) Dark-field optical microscopy images of a Ni-contacted InAs NW device after subsequent thermal annealing steps. The white arrows indicate the remaining InAs NW segments. (f) Ni diffusion length vs the square root of diffusion time for diffusion temperatures of 220, 250, and 280 °C. (g) Diffusivity as a function of the temperature. Inset shows the Arrhenius plot of diffusivity vs $1/T$.

the diffusivity of Ni atoms at 220, 250, and 280 °C by examining the diffusion length, X, as a function of diffusion time (i.e., annealing time), t. An example is shown in Figure 3a−e, for which a Ni-contacted InAs device is annealed at 250 °C for 25, 40, 50, and 60 min in a N_2 environment while being inspected by dark-field optical microscopy after each thermal annealing cycle. Figure 3f shows the linear behavior of X vs $t^{1/2}$ for each diffusion temperature. The observed trend is consistent with the diffusion limited model, that is $X = (Dt)^{1/2}$ where D is the diffusivity of Ni atoms inside InAs NWs (also see Supporting Information, Figure S1). The results suggest that the Ni/InAs alloying reaction is limited by how fast Ni atoms can diffuse in the InAs NW. Once Ni atoms diffuse to the Ni_xInAs/InAs NW interface, the solid reaction of Ni and InAs takes place instantaneously, resulting in sharp epitaxial interfaces. This reaction behavior is similar to the previously explored Ni silicidation of Si NWs.[4] From the diffusion length studies of the Ni/InAs system, diffusion coefficients, $D = 8 \times 10^{-12}$, 3.35×10^{-11}, and 1.13×10^{-10} cm^2/s, were obtained for 220, 250, and 280 °C diffusion temperatures, respectively (Figure 3f). The activation energy is extracted by using the Arrhenius relationship $D \propto e^{-E_a/kT}$, where E_a is the activation energy, k is Boltzmann's constant, and T is the diffusion temperature. From the temperature-dependent diffusivity values, we extract $E_a \sim$ 1.04 eV/atom (Figure 3g).

Notably, Ni diffusivity and Ni/InAs alloying reaction rate are independent of the NW diameter for $d = 20−40$ nm InAs NWs used in this study. This is in distinct contrast to the Ni/Si NW system for which a significant diameter dependence was previously reported by Lu, K.-C., et al. and attributed to the diffusion flux of Ni atoms through the native SiO_2 shell of Si NWs as the limiting reaction step.[4] In that study, Ni NWs, overlapped on the top of Si NWs, were used as the Ni source. In such a system, native SiO_2 is expected between Ni and Si at the point contact interfaces. It was speculated that, as a result, for smaller diameter NWs with smaller contact interface area, a slower injection of Ni atoms is obtained, leading to the observed diameter dependence of the silicidation reaction rate. In our study, however, Ni is evaporated on the end segments of InAs NWs following a HF dip to remove the native oxides (i.e., InO_x and AsO_x) at the interface. As a result, in our study, Ni flux at the contact interfaces is not expected to be the rate-limiting step, which may explain the lack of diameter dependence for Ni diffusivity.

To further shed light on the materials properties of the Ni/InAs system, electrical transport measurements of Ni_xInAs and InAs/Ni_xInAs heterojunction NWs were conducted. First, we extended the diffusion time to form fully metalized Ni_xInAs NWs. The linear $I_{DS}−V_{DS}$ characteristic of Ni_xInAs NW devices, without any dependence on the back-gate voltage, confirms the metallic property of the NWs with ohmic contacts (Supporting Information, Figures S2−S3). From the electrical transport data, resistivity, ρ as a function of diameter is obtained by taking the length and cross-sectional area of NWs into account, as shown in Figure 4a. For NWs with $d > \sim 30$ nm, the resistivity is nearly

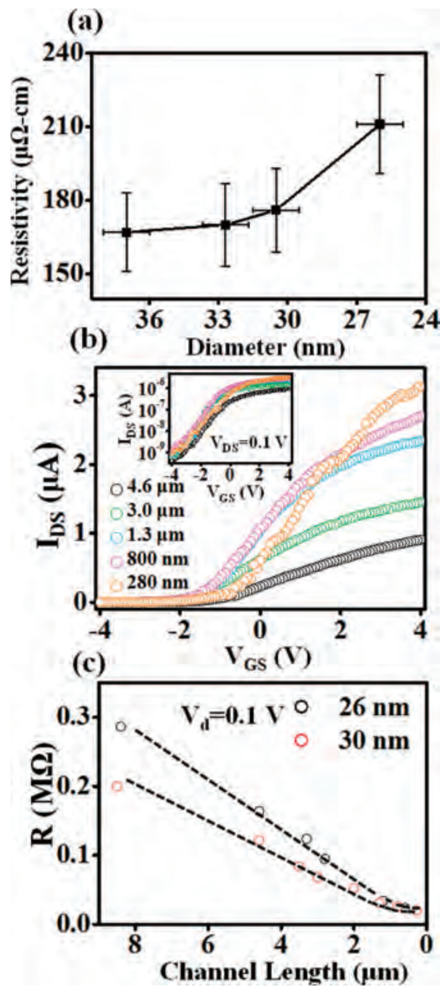

Figure 4. Electrical characteristics of $Ni_xInAs/InAs/Ni_xInAs$ heterojunction and Ni_xInAs NWs. (a) Resistivity of Ni_xInAs NWs as a function of NW diameter. (b) Transfer characteristics ($V_{DS} = 0.1$ V) of a $Ni_xInAs/InAs/Ni_xInAs$ NW FET ($d = 30$ nm) in a back-gated configuration (50 nm SiO_2 gate dielectric) after subsequent annealing steps were used to gradually reduce the length of the InAs NW channel through the formation of Ni_xInAs. Inset shows the corresponding logarithm scale of the $I_{DS}-V_{GS}$ characteristics. (c) The ON-state resistance vs the channel length for 26 and 30 nm InAs NWs after the subtraction of resistance caused by Ni_xInAs electrodes (see Supporting Information, Figure S5).

independent of the diameter with $\rho \sim 167$ $\mu\Omega$·cm. For smaller diameter NWs, however, the resistivity monotonically increases as the diameter is reduced with $\rho \sim 211$ $\mu\Omega$·cm for $d \sim 25$ nm NW (Figure 4a). The resistivity is an intrinsic property, which is directly related to the electron transport properties of the material. The higher resistivity for small diameter NWs may be attributed to the higher surface scattering of the carriers in these high aspect ratio materials. In addition, the durability and reliability tests of Ni_xInAs NWs indicate that a maximum current density of $\sim 10^8$ A-cm^{-2} is attainable before the NW breakage (see Supporting Information, Figure S3), which is comparable to the silicide systems.[5-8]

Additionally, we investigated the electrical properties of the $Ni_xInAs/InAs/Ni_xInAs$ NW heterojunctions, which were configured as back-gated (50 nm thermal SiO_2 gate dielectric) transistors with Ni_xInAs serving as nanoscale contacts and InAs as the channel material. The channel length was tuned by the Ni diffusion time, therefore, enabling a systematic study of the electrical properties as a function of the channel length. An example of a characterized device is shown in Figure 4b for which the $I_{DS}-V_{GS}$ curves were measured after subsequent diffusion steps (250 °C in N_2 ambient) with $L = 4.6-0.28$ μm. For the channel length of $L \sim 4.6$ μm, a peak transconductance, $g_m = dI_{DS}/dV_{GS} = 0.23$ μS at $V_{DS} = 0.1$ V is obtained, which increases to ~ 1.4 μS for the same device when L is reduced to 280 nm. Notably, no significant change in the threshold voltage, V_t, and the OFF current, I_{OFF}, is observed as L is reduced (i.e., following N_2 annealing) to the sub-1 μm regime, which implies that (i) the lack of Ni contamination (i.e., doping) of the InAs channel as the $InAs/Ni_xInAs$ interface is atomically abrupt, and (ii) short channel effects are limited even for this device configuration with 50 nm SiO_2 back-gate dielectric. In contrast, severe short channel effects were observed for the submicron InAs FETs with bulk Ni contacts (fabricated by e-beam lithography), instead of Ni_xInAs NW contacts (see Supporting Information, Figure S4). This result clearly illustrates the advantage of using nanoscale contacts for improved electrostatics, as was also previously reported for Ge/Si NW FETs.[3]

Figure 4c illustrates the extracted resistance, R as a function of L under the "ON" state with $|V_{GS} - V_t| = 4$ V for two different NW diameters ($d = 26$ and 30 nm) after subtracting the resistance of the Ni_xInAs electrodes (see the Supporting Information, Figure S5). The smaller diameter NW exhibits a larger R, which is expected due to the reduced effective channel width. The length-dependent resistance for both NW diameters exhibits a similar behavior, consisting of two distinct regimes (Figure 4c). For $L > 1$ μm, we observe a linear dependence of the resistance on the channel length with a slope of ~ 7.5 kΩ/μm. On the other hand, for $L < 1$ μm, the resistance shows a significantly smaller dependence on the length, approaching the saturation resistance of ~ 38.5 kΩ. This trend suggests an electron mean free path on the order of a few hundred nm, which results in diffusive carrier transport for $L > 1$ μm and quasiballistic/ballistic transport for $L < 1$ μm. This extracted mean free path is consistent with that of the bulk InAs, which was previously reported to be ~ 0.3 μm.[9]

It should be noted that while the annealing gas environment does not significantly impact the diffusivity of Ni (see Supporting Information, Figure S1), it has considerable effects on the electrical properties of the enabled devices. For devices annealed in N_2 and NH_3 ambient, the threshold voltages and the I_{OFF} remain approximately constant as the channel length is reduced. On the other hand, a significant shift in the threshold voltage and reduction of I_{ON}/I_{OFF} is observed for the devices annealed in H_2 environment (see Supporting Information Figure S6). We speculate that this behavior is due to the reduction of surface native oxide layers, such as InO_x or AsO_x, resulting in the change of the surface states or the surface stoichiometry.[10]

In general, to achieve high frequency operation, an underlap between the gate and S/D electrodes is desired to minimize the parasitic capacitances. However, large under-

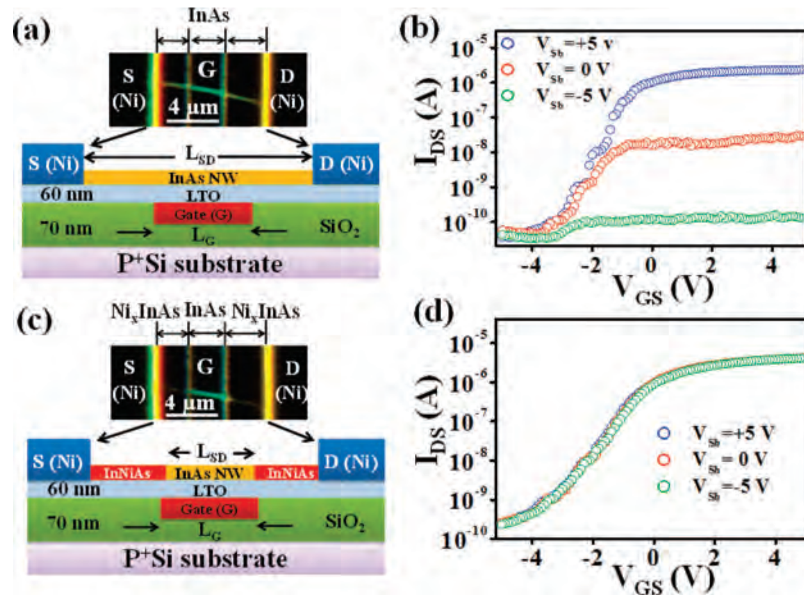

Figure 5. Buried gate InAs NW FETs. (a) Side-view schematic of a buried gate FET with $L_{SD} > L_G$. Upper inset shows the dark-field optical microscopy image of a representative device without annealing. (b) The corresponding $I_{DS}-V_{GS}$ at $V_{DS} = 0.5$ V under different global back-gate (i.e., p+ Si) voltages, V_{sb}. (c) The schematic illustration of the buried gate configuration for after thermal diffusion of Ni to form Ni_xInAs NW contacts. The inset shows the optical image of the same device as (a) but after thermal diffusion of Ni. (d) The corresponding $I_{DS}-V_{GS}$ at $V_{DS} = 0.5$ V under different back-gate voltages, showing minimal dependence of the current on the back-gate voltage.

laps deteriorate the ON currents by inducing parasitic resistances. Therefore, careful design considerations need to be applied for nanoscale devices. To attain low parasitic capacitance, we fabricated buried-gate InAs NW FETs with S/D separation, $L_{SD} \sim 7$ μm, and gate length, $L_G \sim 3$ μm, as shown in Figure 5a. The fabrication process involves (i) drop casting of InAs NWs on p^+Si/SiO_2 (~70 nm thick, thermally grown) substrates, (ii) photolithography to define the buried-gate electrodes, (iii) patterned dry etching of the SiO_2 layer to a depth of ~20 nm with the photoresist layer used as the mask, (iv) electron-beam evaporation of Ti/Pt (~1, 20 nm) bilayer for the gate material, (v) lift-off of the resist, (vi) low temperature chemical vapor deposition of ~60 nm SiO_2, (vii) densification of the oxide at 650 °C for 5 min, and (viii) finally, patterning and metallization of Ni S/D contacts by photolithography and lift-off. In this transistor configuration, the global back-gate is used to electrostatically "dope" the end segments of InAs NWs (underlapped with the buried-gate) into n+ while the buried-gate is used for the channel switching. The device operates similar to conventional MOSFETs with heavily doped S/D contacts. The ungated regions, however, induce a relatively large parasitic resistance. Additionally, the ON-current depends on the global back-gate voltage (Figure 5b). A more optimal device configuration involves using metallic NWs with low resistivity in the underlap regions. The use of metal contacts, however, is not attractive for Si devices due to the Schottky barriers encountered at the interfaces, resulting in lower carrier injection efficiencies. In contrast to Si, however, it is well established that ohmic metal contacts for electron transport, free of any Schottky barriers, can be readily achieved for InAs due to the pinning of the surface Fermi level deep into the conduction band. This presents an opportunity to incorporate metal nanocontacts with InAs NWs to enable low parasitic resistances, ohmic contacts, and yet improved electrostatics. To attain such nanocontacts, we utilized the InAs metallization process by annealing Ni-contacted InAs NW FETs in N_2 at 250 °C for 45 min, during which Ni atoms diffuse from the Ni pads and into the InAs nanowire to form metallic Ni_xInAs contacts. The diffusion time was adjusted based on the diffusivity of Ni at 250 °C (Figure 3f) and the length of the underlapped regions. The electrical properties for such a device are shown in Figure 5d, exhibiting minimal dependence on the global back-gate voltage, V_{sb}. In addition, the ON-current is enhanced from ~2.3 to ~4.1 μA due to the lower resistivity of Ni_xInAs as compared to InAs. The result confirms the formation of metallic Ni_xInAs in the underlapped regions through the solid source reaction, and presents a novel device structure for future nanoscale InAs transistors.

In summary, we have described the first report of the formation of crystalline Ni_xInAs/InAs/Ni_xInAs and Ni_xInAs NWs. The fundamental reaction kinetics of the alloying of InAs NWs with Ni is explored. The Ni diffusivity is independent of the NW diameter (for $d = 20-40$ nm) and the diffusion ambient (N_2, NH_3, and H_2). Ni_xInAs exhibits a modest resistivity of 167−211 $\mu\Omega$·cm for $d = 20-40$ nm and enables ohmic contacts to chemically intrinsic InAs NWs with atomically abrupt interfaces. The resistivity of Ni_xInAs is independent of the NW diameter for $d > \sim 30$ nm but increases as the diameter is reduced to sub-30 nm regime, which is attributed to the enhanced surface scattering. By controlling the diffusion time and temperature, the channel length of InAs NW FETs is readily tuned, enabling systematic studies of the $I-V$ characteristics as a function of InAs channel length, and shedding light on the intrinsic electron

transport properties of InAs. Finally, InAs transistors with buried local gates that underlap Ni S/D contacts are fabricated. The underlapped regions are controllably metalized through the formation of Ni_xInAs to enable ohmic nanocontacts to the InAs channel with minimal parasitic capacitances and resistances. This work could have important implications for future nanoscale transistors based on InAs channel materials.

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Note Added after ASAP Publication: There was an error in Figure 3 in the version published November 3, 2008; the corrected version was reposted November 21, 2008.

Supporting Information Available: The Ni diffusion length studies for different nanowire diameters and diffusion ambient, $I-V$ characteristics of Ni_xInAs NWs, electrical properties of short-channel InAs NW FETs with nanoscale and bulk contacts, and the $I-V$ characteristics of InAs NW FETs annealed in H_2. This material is available free of charge via the Internet at http://pubs.acs.org.

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Supporting Information

Formation and Characterization of $Ni_xInAs/InAs$ Nanowire Heterostructures by Solid Source Reaction

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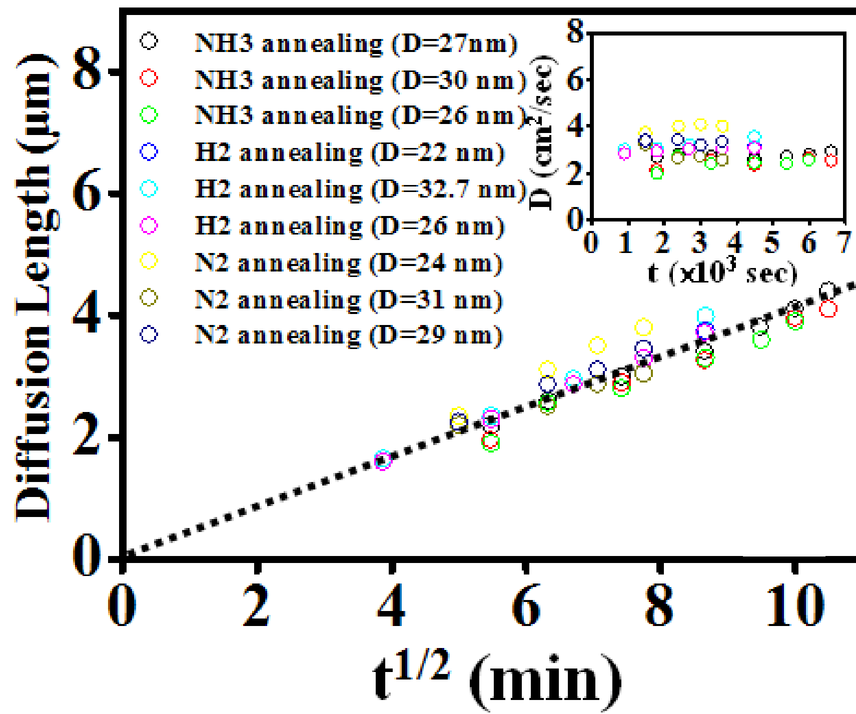

Figure S1. Ni diffusion length vs the square root of diffusion time at annealing temperature of 250 ºC for different nanowire diameters and diffusion environments, demonstrating that the diffusivity does not depend on the diffusion ambient or the NW diameter for the diameter range explored in this study.

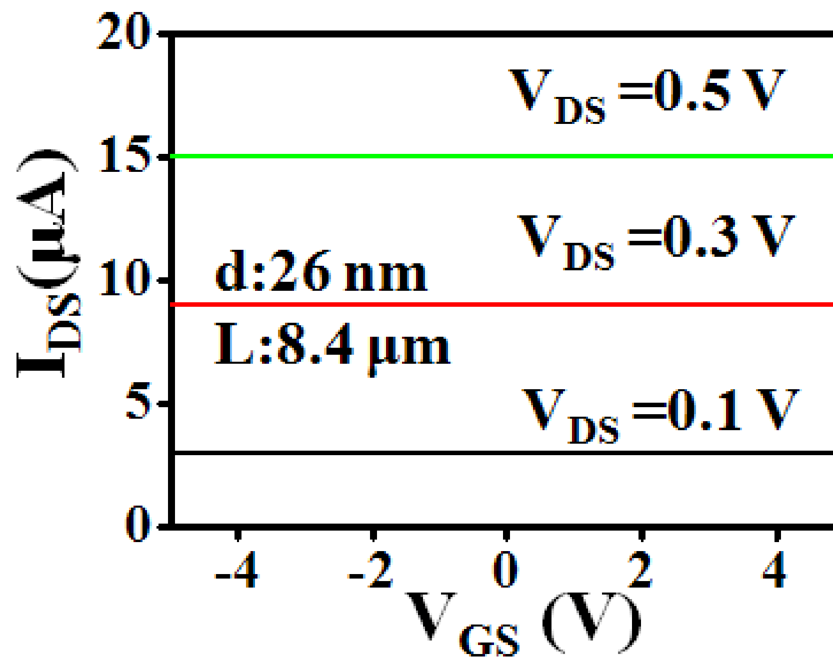

Figure S2. The I_{DS}-V_{GS} behavior for a Ni_xInAs NW at V_{DS}=0.1, 0.3, and 0.5 V, exhibiting minimal dependence of current on the gate voltage, and illustrating the metallic behavior of the NW.

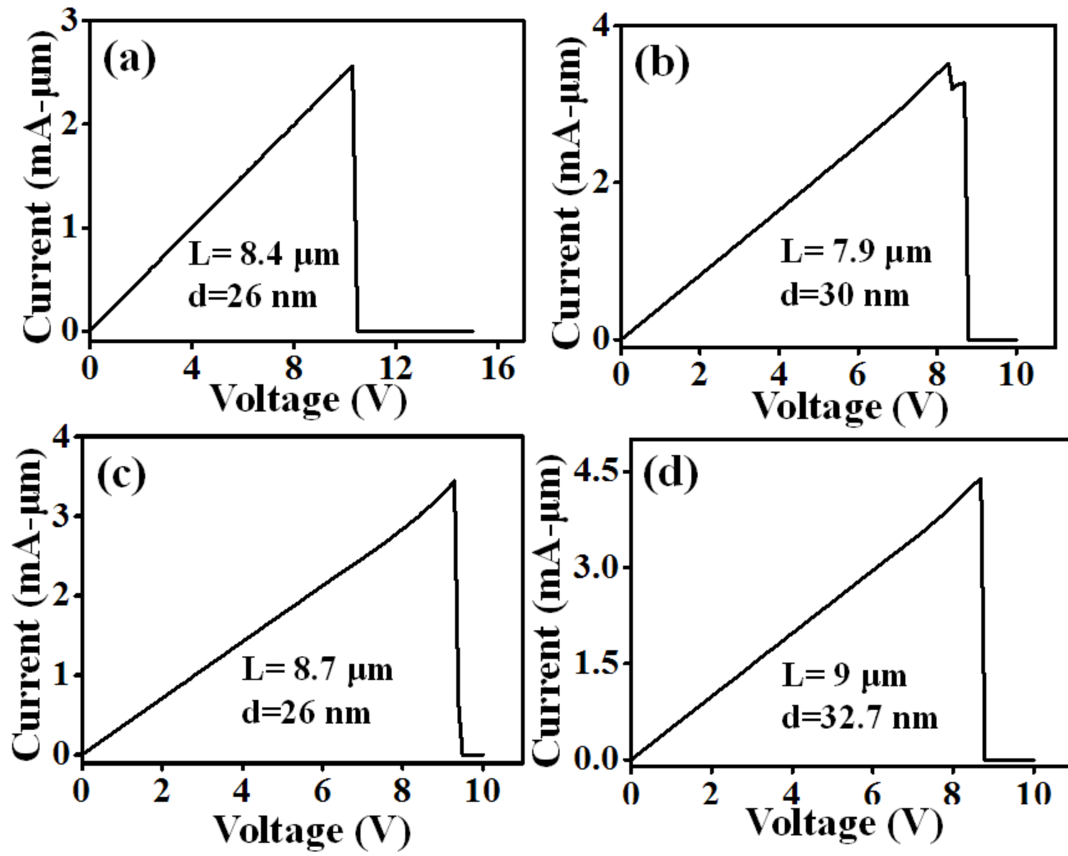

Figure S3. The channel length normalized current vs voltage for different diameter Ni_xInAs NWs.

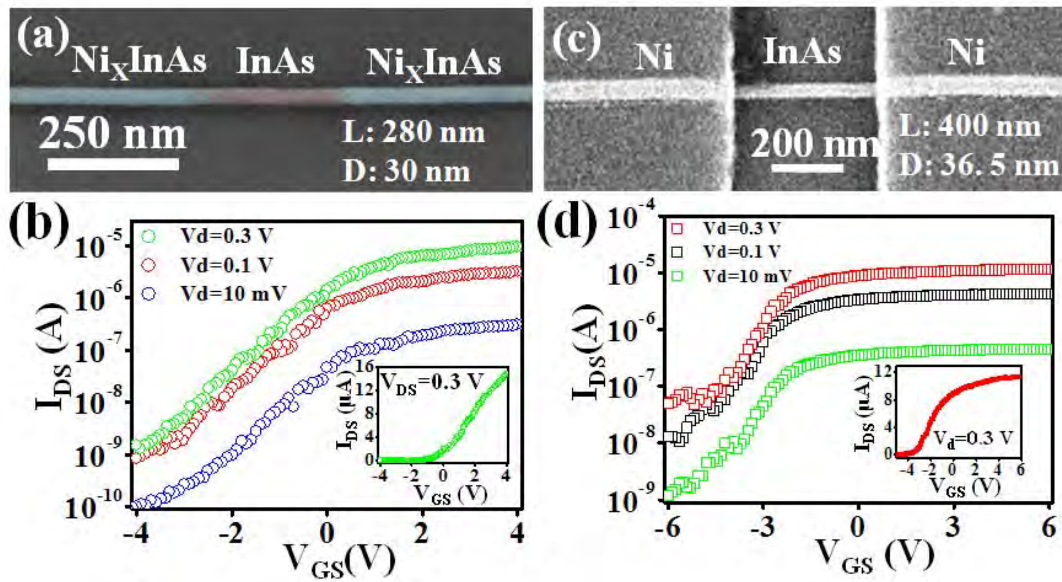

Figure S4. (a) SEM image of a short channel, back-gated FET formed by using the InAs metallization approach, with nanoscale Ni_xInAs contacts. The channel length is ~280 nm. (b) The corresponding I_{DS}-V_{GS} behaviors at V_{DS}=10 mV, 0.1 V and 0.3 V. Inset shows the linear scale I_{DS}-V_{GS} at V_{DS}=0.3V. (c) SEM image of a short channel, back-gated FET fabricated by electron-beam lithography, with bulk Ni contacts. The channel length is ~400 nm. (d) The corresponding I_{DS}-V_{GS} behaviors at V_{DS}=10 mV, 0.1 V, and 0.3 V. Inset shows the linear scale of I_{DS}-V_{GS} at V_{DS}=0.3V. It is clearly evident that the FET with bulk contacts exhibits ~2 orders of magnitude higher I_{OFF} (~10^{-7} vs. 10^{-9} A) due to short channel effects.

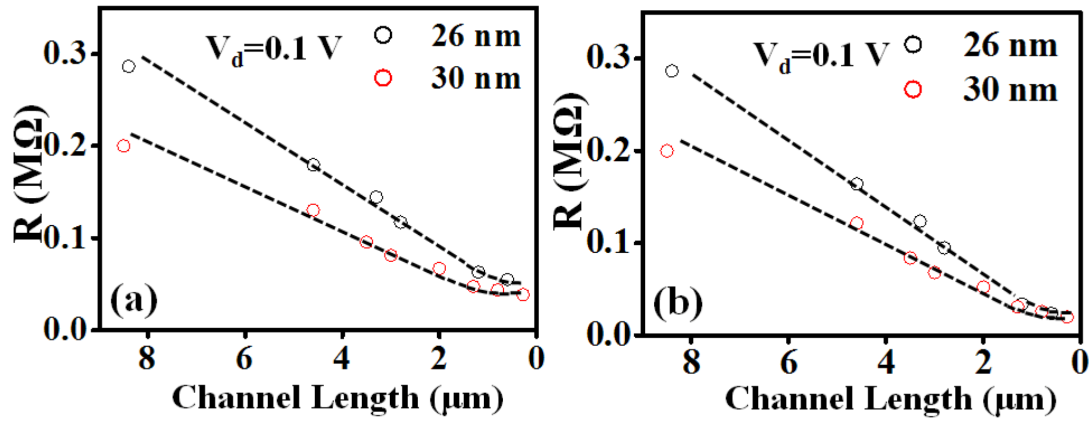

Figure S5. ON-state resistance vs. the channel length for 26 and 30 nm InAs NWs achieved by subsequent annealing/diffusion steps (a) before and (b) after subtraction of resistance caused by Ni_xInAs electrodes. The resistance of Ni_xInAs contacts was estimated from our measured resistivity values (see Fig. 4(a)).

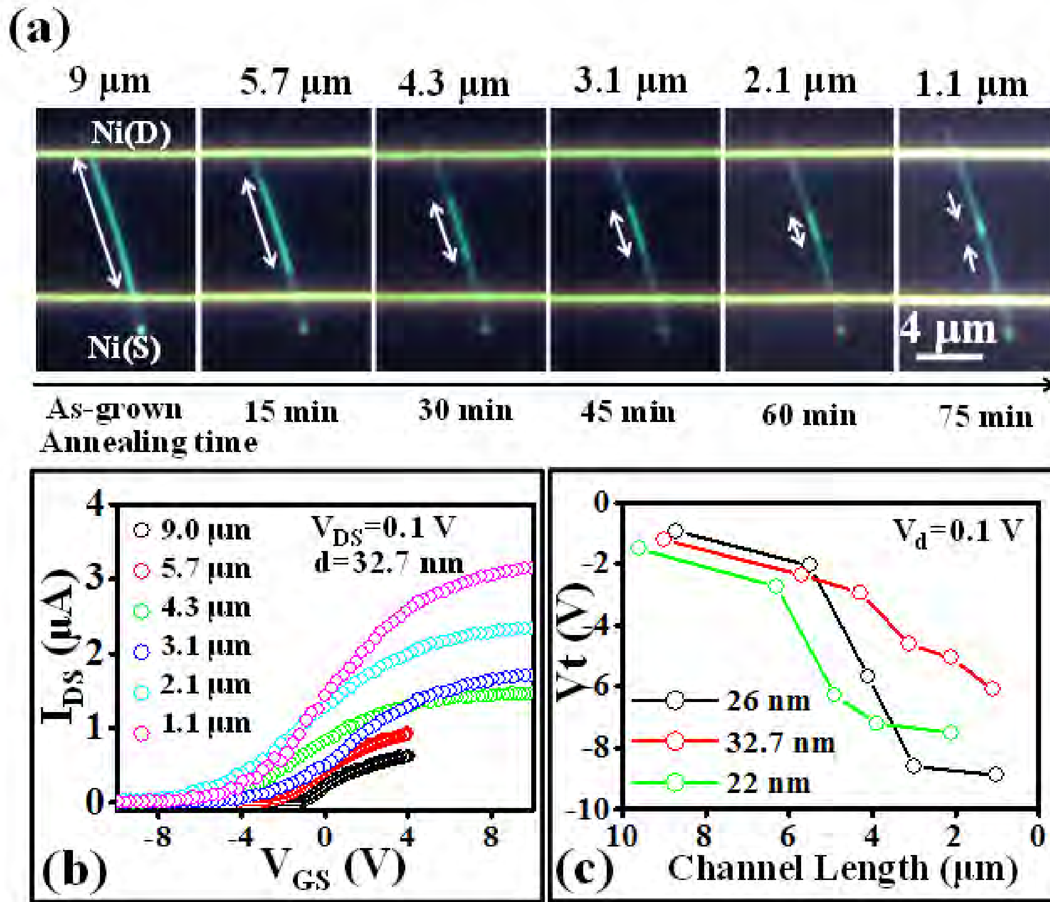

Figure S6. Ni/InAs alloying reaction by thermal annealing at 250ºC in H_2 environment. (a) The dark field optical microcopy images after subsequent annealing steps, showing the formation of Ni_xInAs. (b) The I_{DS}-V_{GS} characteristics at V_{DS}=0.1 V for different channel lengths, demonstrating a shift in the threshold voltage as the channel is reduced. (c) The threshold voltage vs the channel length for three different nanowires. In contrast to InAs NW devices that were annealed in N_2, H_2 annealed devices exhibit a major shift in V_t as a function of diffusion time (i.e., diffusion length).