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Review Article

III–V Nanowires: Synthesis, Property Manipulations, and Device Applications

Ming Fang,[1] Ning Han,[1,2] Fengyun Wang,[3] Zai-xing Yang,[1] SenPo Yip,[1,2] Guofa Dong,[1] Jared J. Hou,[1,2] Yulun Chueh,[4] and Johnny C. Ho[1,2]

[1] *Department of Physics and Materials Science, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong*
[2] *Shenzhen Research Institute, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong*
[3] *Cultivation Base for State Key Laboratory, Qingdao University, No. 308 Ningxia Road, Qingdao, China*
[4] *Department of Materials Science and Engineering, National Tsing Hua University, No. 101 Section 2 Kuang-Fu Road, Hsinchu 30013, Taiwan*

Correspondence should be addressed to Johnny C. Ho; johnnyho@cityu.edu.hk

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III–V semiconductor nanowire (NW) materials possess a combination of fascinating properties, including their tunable direct bandgap, high carrier mobility, excellent mechanical flexibility, and extraordinarily large surface-to-volume ratio, making them superior candidates for next generation electronics, photonics, and sensors, even possibly on flexible substrates. Understanding the synthesis, property manipulation, and device integration of these III–V NW materials is therefore crucial for their practical implementations. In this review, we present a comprehensive overview of the recent development in III–V NWs with the focus on their cost-effective synthesis, corresponding property control, and the relevant low-operating-power device applications. We will first introduce the synthesis methods and growth mechanisms of III–V NWs, emphasizing the low-cost solid-source chemical vapor deposition (SSCVD) technique, and then discuss the physical properties of III–V NWs with special attention on their dependences on several typical factors including the choice of catalysts, NW diameters, surface roughness, and surface decorations. After that, we present several different examples in the area of high-performance photovoltaics and low-power electronic circuit prototypes to further demonstrate the potential applications of these NW materials. Towards the end, we also make some remarks on the progress made and challenges remaining in the III–V NW research field.

1. Introduction

In the past decades, semiconductor nanostructures have attracted numerous research attentions due to their unique fundamental physical properties as well as the great potentials for various technological applications [1–6]. In particular, most III–V semiconductor nanowires (NWs) have direct bandgap which can be controllably manipulated over a wide range by tailoring their stoichiometry, being advantage for full-spectrum photovoltaics. Many of these NWs (e.g., InAs) also hold impressively high carrier mobilities for high-speed devices which cannot be easily achieved in silicon and other nanostructures [7, 8]. At the same time, these NW materials also show a number of key advantages over their bulk counterparts. For example, downscaling of the semiconductor materials into NW crystals would render them mechanical flexibility, making them ideal active materials for future flexible electronics [9–14]. Likewise, their remarkably large surface-to-volume ratios as well make the NWs attractive for the high-performance sensors. With the unique one-dimensional structure, miniaturized co-axial core-multi-shell heterojunctions could also be produced, which further improves the application potentials of the NWs [15]. Yet, for the practical implementations, these intriguing NW materials with the better understanding about their syntheses, properties manipulations and low-cost integrations are still needed [16–22].

The purpose of this work is to present a general overview of the recent development in III–V NWs with the focus on their cost-effective synthesis, corresponding property

manipulation as well as the relevant low-operating-power device applications. We will first go over the synthesis methods and investigate the growth mechanisms of III–V NWs, emphasizing in the low-cost solid-source chemical vapor deposition (SSCVD) technique. Various physical properties of III–V NWs would then be assessed with the special attention in their dependences on several typical factors including the choice of catalysts, NW diameters, surface roughness and surface decorations, and so forth. In the later stage, different examples in the area of high-performance photovoltaics and low-power electronic circuit prototypes would also be demonstrated through the device integration of these NWs.

2. Synthesis of III–V NWs

2.1. The SSCVD Growth Method. Generally, semiconductor NWs can be synthesized by employing metal nanoclusters as catalysts via vapor-liquid-solid (VLS) and/or vapor-solid-solid (VSS) growth mechanisms [15, 23–25]. In a VLS growth, vapor-phase precursors are introduced at temperature above the eutectic point of the metal-semiconductor system, resulting in liquid droplets of the metal-semiconductor alloy. Continuously feeding the precursors leads to the supersaturation of catalytic droplets, upon which the semiconductor material starts to nucleate out of the melt and grow into crystalline NWs [26]. Unlike the VLS mechanism, in VSS, the metal nanoclusters exit as solid particles. It is believed that the particles can provide low-energy interface for trapping the precursor materials and yield higher epitaxial growth rates than elsewhere on the substrate [27]. Specifically, various techniques have been hired to generate vapor-phase precursors for the growth of NWs, including chemical vapor deposition (CVD) [23], pulsed laser ablation [28] and molecular beam epitaxy (MBE) [29]. Among all, a CVD growth method utilizing the conventional tube furnace and solid powder source, namely solid-source CVD, has been widely explored in recent years for the growth of various III–V NWs due to its relatively low setup and operating cost, simple growth procedures and importantly no involvement of toxic gas precursors, as compared to other sophisticated growth systems such as MBE and metal-organic CVD. Figure 1 depicts the typical schematic illustration of the SSCVD growth setup. Source powder is put at the upstream of a two-zone tube furnace, while hydrogen is used as a carrier gas to transport the evaporated source material to the downstream, and a substrate pre-coated with catalysts is positioned at the downstream for the NW growth [25, 30–32]. Here, we discuss the applications of this SSCVD method in the syntheses of different NW materials.

2.2. Synthesis of P- and As-Based NWs. Phosphorus (P)- and arsenic (As)-based III–V NW materials have moderate bandgaps and thus show good photon-response to visible and/or infrared lights as well as excellent on/off ratio when configured into field effect transistors (FETs), holding great potentials for application in future electronics and optoelectronics. MBE and MOCVD methods were typical adopted for the NW growths following the VLS and/or (VSS)

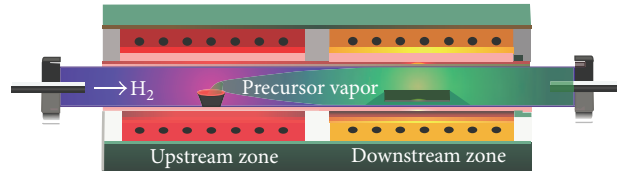

Figure 1: Schematic representation of the typical SSCVD setup and the growth process. Not drawn in scale. Reproduced from [32] with permission from The American Chemical Society.

growth mechanisms; however, single-crystalline substrates are typically employed as the underlying templates for the epitaxial growth of such NWs, which could result in the relatively low growth yield of NWs as well as high cost, restricting the subsequent device integration for certain applications. Alternatively, applying the SSCVD method with metal (Au, Ni, or others) nanoclusters as catalysts, high-quality NWs such as InP and InAs could be easily synthesized on amorphous Si/SiO_2 substrates with high density, via VLS or VSS mechanisms [31, 35].

Although the SSCVD method is a versatile tool for the NW growth, technical modifications are still needed to make it applicable to certain systems, especially for the synthesis of arsenic (As)-based ternary NW materials. For example, for the growth of InGaAs NW, it is difficult to obtain high-quality NW through the standard SSCVD method. In this regard, we developed a two-step growth method in order to overcome this growth challenge [18]. As compared to the conventional single-step method, the two-step approach has an additional nucleation step at a higher temperature before the regular growth step. As shown in Figure 2(a), for a conventional single-step growth, the grown NWs exhibit kinked morphologies with severe surface over-coating. This may be ascribed to uneven growth rate at the catalyst-NW interfaces due to the co-existence of some solid phase in the catalyst droplets given that the temperature between the catalytic eutectoids and the NW growth are similar. On the other hand, when a two-step method is used, NWs are grown in a relatively straight manner and long, without significant surface over-coating, because of the minimization in the chances of solid phase formation within the catalysts (Figure 2(b)). Notably, utilizing this two-step method, bandgap tunable $In_xGa_{1-x}As$ NWs with different chemical compositions can also synthesized by manipulating the source powder mixture ratio and appropriate growth parameters [41].

Moreover, the two-step growth process is also adopted to achieve single-crystalline GaAs NWs where an initial high temperature nucleation process is employed to ensure the formation of high Ga supersaturated Au-Ga alloy seeds, which yields in long (>60 μm) and thick (>80 nm) NWs with the minimal defect concentrations and uniform growth orientations [33]. To further verify the crystal quality difference between these two growth techniques (one-step versus two-step), room temperature photoluminescence (PL) and Raman spectroscopy are performed. As presented in Figure 2(c1), it is clear that the two-step grown NWs have

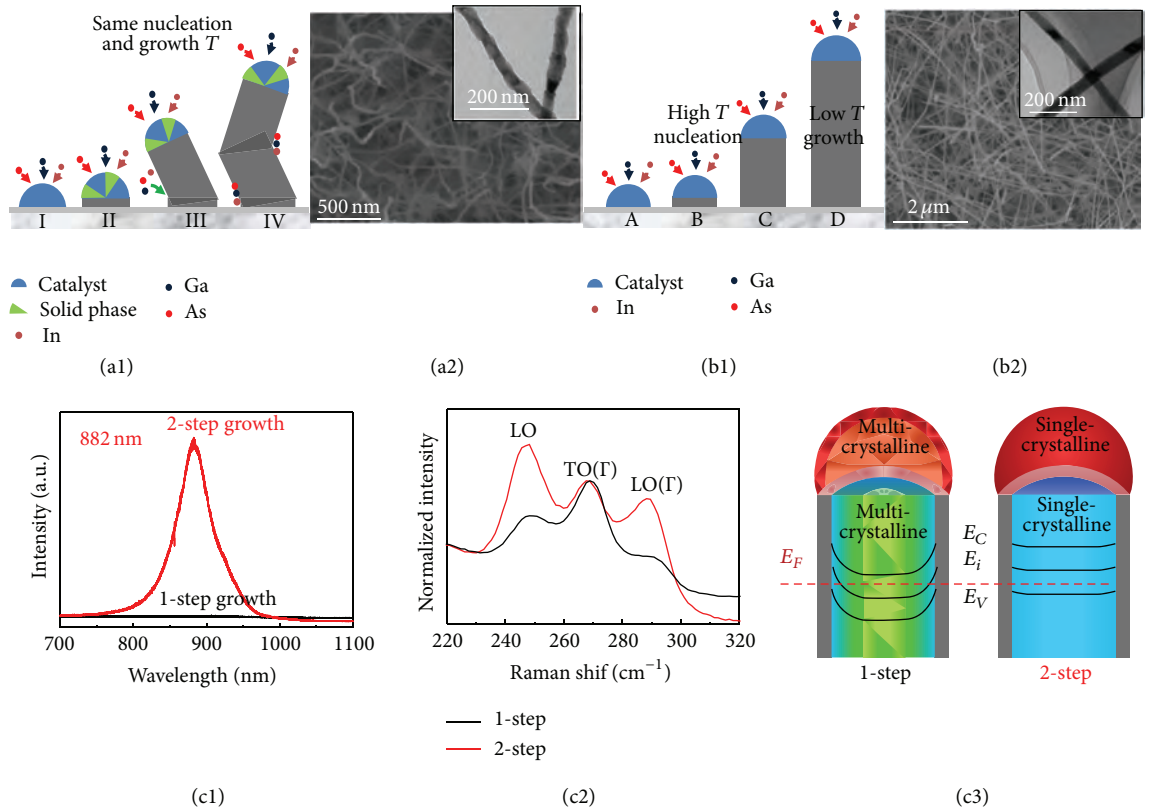

FIGURE 2: (a) Single-step growth method. (a1) Schematic illustration of growth mechanism of the single-step method, demonstrating the kinked morphology and surface coating during the NW growth; (a2) SEM and (inset) TEM images of the NWs grown by the single-step method. (b) Two-step growth method. (b1) Schematic illustration of growth mechanism of the two-step method; (b2) SEM and (inset) TEM images of the NWs grown by the two-step method. (c) Crystal defect characterization between the single- and two-step grown GaAs NWs. (c1) Room temperature PL spectra, showing a good crystal quality of the two-step grown NWs, lacking nonradioactive recombination centers; (c2) Raman spectra with a lower LO(Γ)/TO(Γ) peak intensity ratio indicating the existence of arsenic precipitates in the single-step grown NWs; (c3) Cross-sectional view of NWs with the corresponding crystal quality and equilibrium energy band diagram at the zero gate bias. Reproduced from [18, 33] with permission from The American Chemical Society.

a PL peak at ~882 nm (~1.41 eV), which is consistent to the bandgap of bulk zincblende GaAs. Importantly, the single-step NWs do not give any luminescence even after surface passivation, indicating that the quenched PL mainly comes from the presence of crystal defects in the single-step growth. Also, based on the Raman spectra (Figure 2(c2)), the wider and lower relative peak intensity of LO(Γ) in the single-step NWs probably originate from the related crystal defects such as As precipitates in the NWs. As will be discussed later, these NWs would exhibit distinct conducting behavior with the n-type characteristics in single-step NWs versus p-type features in two-step NWs due to the different degrees of crystallinity (Figure 2(c3)).

2.3. Synthesis of Sb-Based NWs. Antimony (Sb)-based NW materials are as well intriguing owing to their narrow direct bandgap and excellent carrier mobilities, with InSb and GaSb having the highest electron (n-type) and hole (p-type) mobility, respectively, among all III–Vs, which make them ideal materials for field-effect transistors (FETs), quantum devices, thermoelectrics and long-wavelength detectors, and so forth [42–48]. In addition, given that the high performance n-type NWs (such as InAs and InGaAs) have been successfully demonstrated [7, 8, 11, 18, 41], the synthesis of p-type NWs is particularly important for the practical design and implementation of NW based CMOS electronic circuits. However, the growth of high-quality III-Sb NWs is still challenging because of the tendency of the constituent Sb to aggregate on top of the growing layer without being incorporated into the NW growth. Recently, our group has demonstrated a successful synthesis technique utilizing Au nanoclusters as the catalysts to achieve high density GaSb NWs on amorphous Si/SiO_2 substrates via the SSCVD method. By adjusting the source temperature, growth time and altogether with the carrier gas flow rate, a Sb-supersaturated environment is expected to be induced, which are favorable for the growth of high-quality GaSb NWs. In this way, the obtained NWs are crystalline and stoichiometric with uniform diameters as well as minimal surface coatings. When configured into FETs, the NWs exhibit respectable p-channel device characteristics with the peak hole mobility of ~30 $cm^2\ V^{-1}\ s^{-1}$ and effective hole concentration of ~$9.7 \times 10^{17}\ cm^{-3}$ [32].

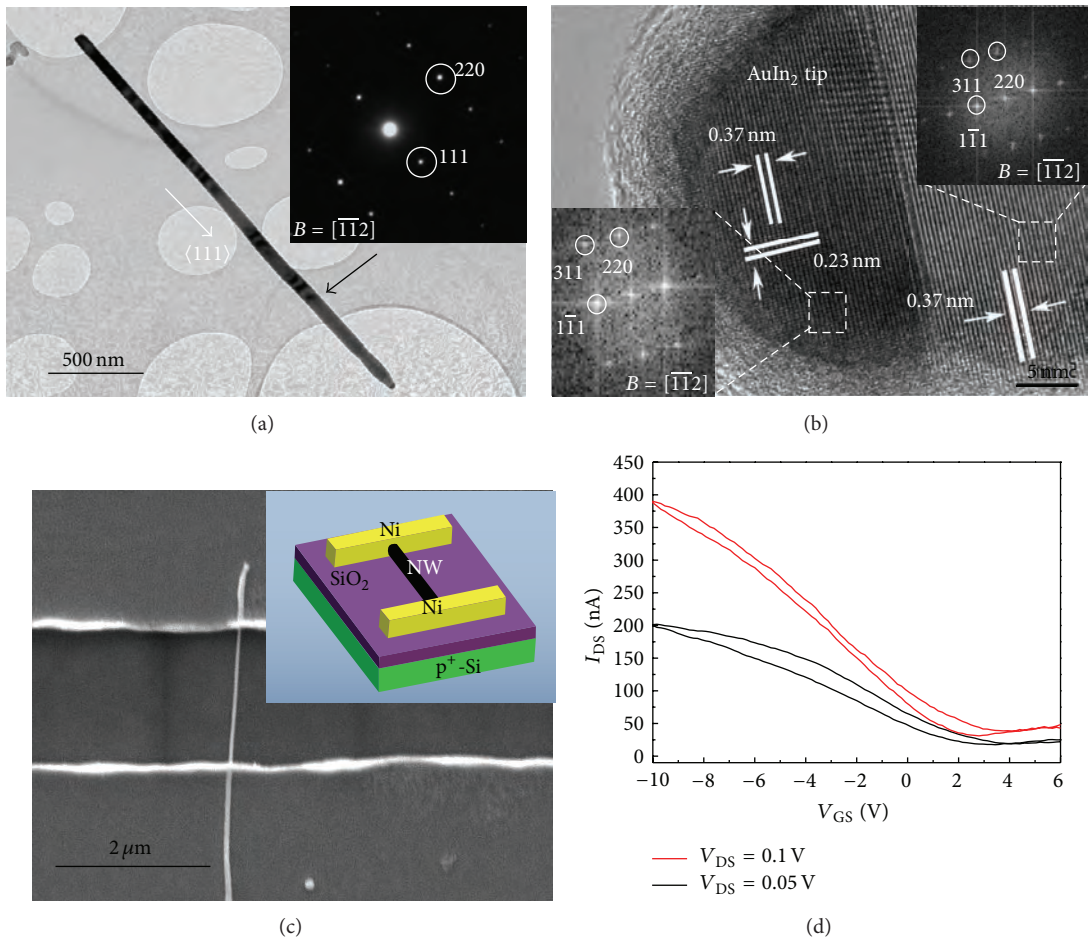

FIGURE 3: (a) TEM and SAED images of a representative p-InSb NW grown under the optimal condition; (b) HRTEM image at the tip region of the same NW. Inset shows the corresponding FFT images; (c) SEM image and (inset) schematic of a back-gated InSb NWFET with Ni metal contacts; (d) transfer and output characteristics of the typical NW FET with the channel width of ~55 nm and length of ~1.8 μm. Reproduced from [34] with permission from The Royal Society of Chemistry.

In addition to the intrinsically p-type NWs, *in-situ* doping during the growth is another feasible way to obtain the p-type conductivity in NWs. For example, we have achieved this p-type doping in the synthesis of InSb NWs via the SSCVD method by intentionally adding carbon powders into the InSb source [34]. The grown NWs exhibit excellent crystallinity (Figures 3(a) and 3(b)) and uniform stoichiometric composition along the entire length of the NWs. Due to the *in situ* carbon-doping, the NWs show high-performance p-type transport properties with the peak hole mobility of 140 $cm^2\,V^{-1}\,s^{-1}$ when configured into FETs (Figures 3(c) and 3(d)). Notably, high electrically active carbon concentrations of $\sim 7.5 \times 10^{17}\,cm^{-3}$ are achieved which are essential for compensating the electron-rich surface layers of InSb to enable the heavily p-doped and high-performance device structures.

3. Manipulations of NW Properties

Materials at nanoscale often exhibit novel properties which are lacked in bulk materials due to the quantum confine effect as well as large surface-to-volume ratio. Such nano-effects are particularly evident in semiconductor NW systems. Many factors, such as the choice of catalyst, NW diameters and surface roughness may have noticeable influence on the properties of NWs. Here, we discuss these factors in details and demonstrate the rational utilization of them to achieve manipulation of the NW properties.

3.1. Influences of the Catalyst Choice on Electronic Transport Properties of NWs. For the NW growth, either via VLS or VSS mechanism, metallic catalysts are always employed. The choice of catalyst material is very important as it could not only influence the composition and morphology, but also affect the electronic transport properties via *in-situ* doping (often unintentional) and defect/vacancy formation. For instance, InAs NWs are often synthesized by the SSCVD method using different metal nanoclusters (e.g., Ni and Au) as catalysts. It is found that the NW morphology as well as the transport properties has strong dependences on the choice of the catalyst [35]. The Ni catalyzed NWs were relatively straight and uniform on substrates, in which

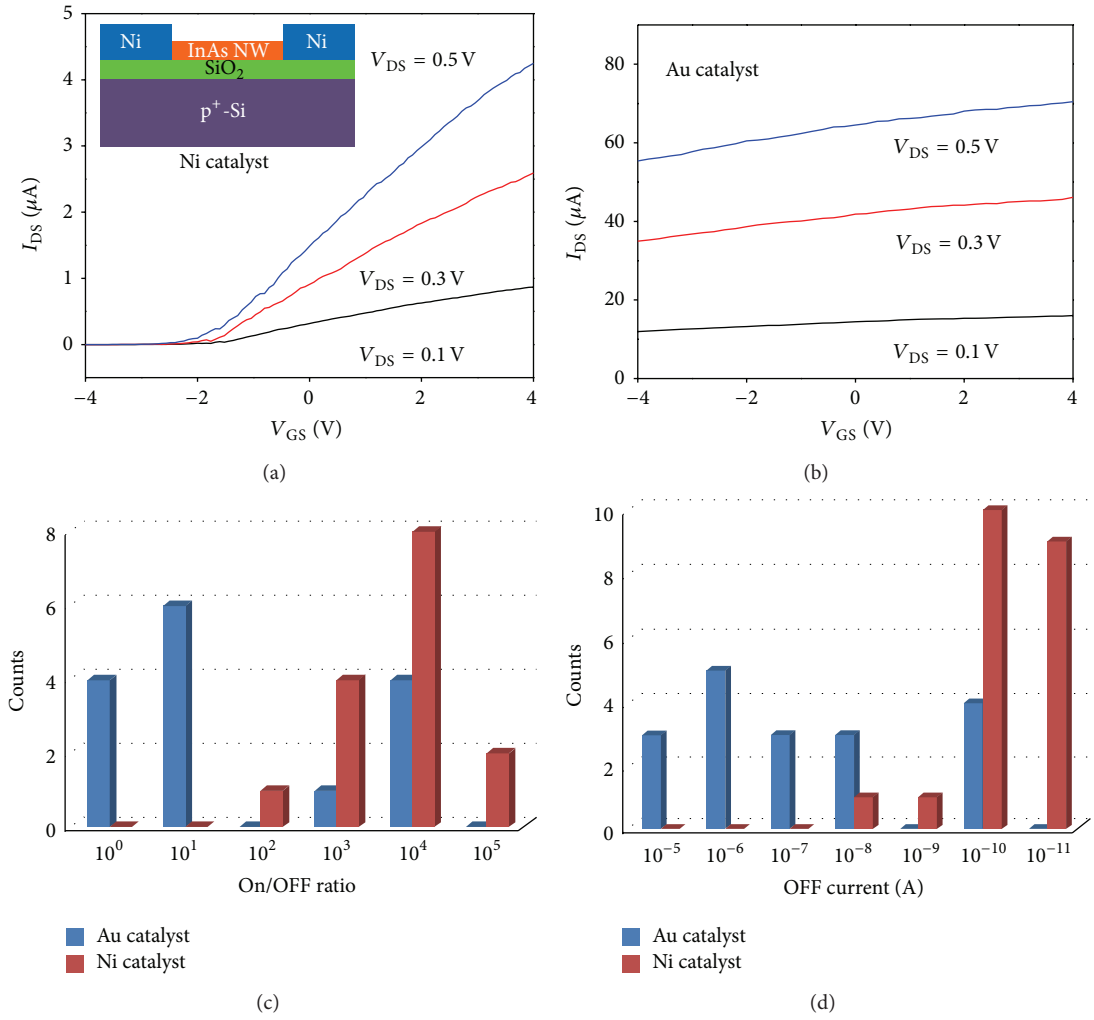

FIGURE 4: I_{DS}-V_{GS} curves of InAs NWs FETs at V_{DS} = 0.1, 0.3 and 0.5 V grown from (a) Ni and (b) Au as catalysts. Statistical results of (c) I_{ON}/I_{OFF} ratios and (d) OFF currents extracted from 100 devices based on Ni-catalyzed and Au-catalyzed InAs NWs, respectively. Reproduced from [35] with permission from the PCCP Owner Societies.

~98% of the NWs exhibit a very unvarying n-type behavior with strong gate dependence, giving the impressive OFF current (~10^{-8}–10^{-10} A) with the maximum $I_{ON}/I_{OFF} > 10^4$ (Figures 4(a), 4(c) and 4(d)). On the other hand, the Au-catalyzed NWs show tapered morphology and unstable plus non-uniform electrical properties with ~80% of the NWs exhibiting weak gate dependence characteristics (Figures 4(b), 4(c) and 4(d)). The unstable and non-uniform electrical transport performance is ascribed to the non-stoichiometric composition of the NWs due to the different segregation or NW growth schemes from the Au catalyst. The lateral growth or sidewall over-coating may induce intrinsic defects such as interstitials or vacancies, resulting in the unstable and non-uniform electrical properties of grown NWs.

3.2. Diameter-Dependence of NW Properties. Diameter is another key feature for the NW characterization. Different diameter implies different surface-to-volume ratio, which could significantly influence the electronic properties of NWs [49–54]. It is well known that for III–V NWs, there always exists an amorphous oxide shell over the core NW material when it is exposed in ambient environment. In GaAs NWs, these oxide shells could deplete the carrier density in the NWs by contributing abundant acceptor-like interface trapping states and/or defects, in which the depletion space-charge region can extend deep inside the NWs. Our study further reveals that this effect could result in distinct electronic properties of NWs when they have different diameters. As depicted in Figure 5 [36], for large diameters ($d > 70$ nm), the NWs give intrinsically n-channel conduction behavior because of the minimal space-charge depletion effect, whereas for NWs with small diameters ($d < 40$ nm), owing to the enhanced surface-to-volume ratio, the contribution coming from the oxide trap states becomes pronounced and yields full depletion of the NWs which further exhibit inverted p-channel behavior. For NW diameters between $40 < d < 70$ nm, ambipolar conduction in lower current magnitude is observed. Besides to provide a facile method

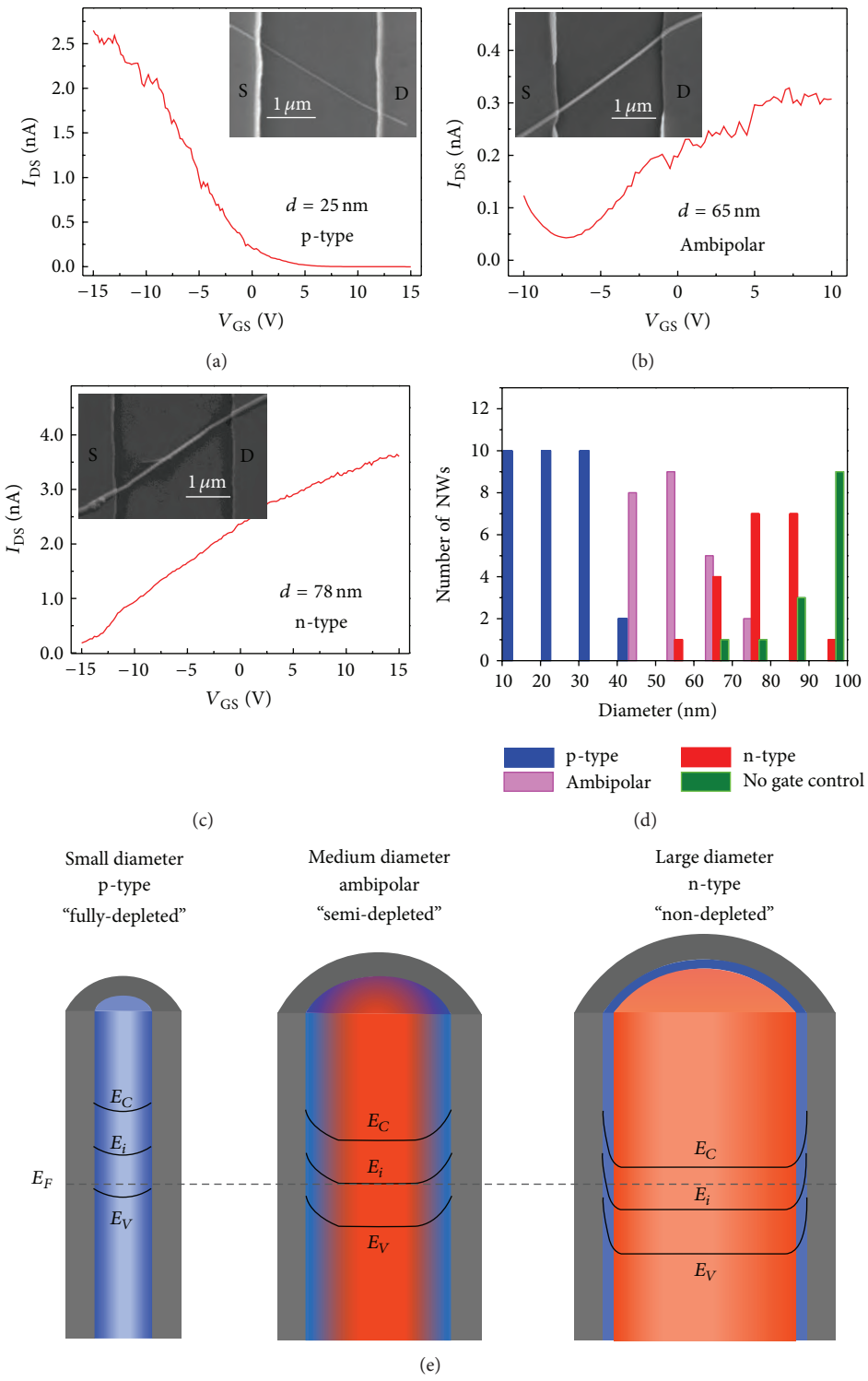

FIGURE 5: Typical I_{DS}-V_{GS} curves of GaAs NW FETs based on different NW diameters (V_{DS} = 2 V): (a) p-type characteristic (d = 25 nm), (b) ambipolar conduction (d = 65 nm), (c) n-type characteristic (d = 78 nm), and (d) statistics of the p- to n-type transition with increasing NW diameters in the range of 10–100 nm. (e) Cross-sectional view of GaAs NWs with different diameters and the corresponding equilibrium energy band diagram at zero gate bias. Reproduced from [36] with permission from The American Chemical Society.

for manipulating the conduction type (p-type versus n-type) of NWs, this study also suggests that the diameter scaling of NWs not only affects their carrier mobility and gate control efficiency [7], but also alters their electronic transport via the different contributions of the native-oxide-induced space-charge depletion; therefore, careful device design considerations are required for achieving the optimal device performances.

From the viewpoint of device design, miniaturization of NW diameters is always helpful to improve the gate electrostatic control as well as to lower the off-state current. On the other hand, diameter scaling of NWs would inevitably introduce more surface scattering and higher surface carrier recombination, which are detrimental to the carrier mobility of NW transistors. This way, investigating the dependence of carrier mobility on NW diameter is essentially important for future device geometrical design and optimization. Two-step grown $In_{0.7}Ga_{0.3}As$ NWs are chosen for this study due to their intrinsically higher electron mobility. By exploring the electrical characteristics of NW transistors, the peak electron field-effect mobility is found to decrease as the NW diameter reduces, with the peak mobility of ~4500, 3000, and 1400 $cm^2\ V^{-1}\ s^{-1}$ at room temperature for representative thick (d = 41.9 nm), medium (d = 32.4 nm), and thin NWs (d = 19.3 nm), respectively (Figure 6), which experimentally confirms that diameter scaling of NWs could lead to carrier mobility degradation. The same dependency is also observed at low-temperature current-voltage (I-V) measurement [37], which eliminates the influence of acoustic phonon scattering and thermal activated surface/interface traps in this diameter scaling, revealing the impact of surface roughness scattering (will be discussed later) on the mobility degradation for miniaturized NWs.

3.3. Surface Roughness Effects. Theoretically, the surface roughness could induce significant changes in the NW electronic band structure and modulate its transport properties, including carrier mean free paths, mobilities and others [55–57]. In our study, we use high-quality InAs NWs as models to explore the electron mobility dependence on the surface roughness. The NW dimensions and surface conditions are characterized by AFM, and the electrical characteristics of the NWs are investigated by configuring them into back-gate FET devices [38]. Figure 7(a) displays the statistics of the peak electron mobility of NWs as a function of surface roughness with different diameter ranges. One can see that the tendency of degradation of electronic mobility goes with the increase of NW surface roughness. Low-temperature electrical measurements are also performed in order to further elucidate the role of surface roughness among all possible scattering mechanisms by decoupling the influence of phonon scattering and thermal activated surface/interface traps. As shown in Figure 7(b), all mobility values with different surface roughness are improved at 77 K because of the frozen of all phonon modes and surface traps; however, this improvement is more profound for smooth NWs, highlighting the dominant role of surface roughness for the observed mobility degradations. This mobility degradation agrees well with the theory that surface roughness can easily induce changes in the local electronic band structures, which act like scattering potentials that scatter carriers moving in the NW, reducing the mean free time and mobility consequently [55–58].

3.4. Metal-Cluster-Decoration for Manipulations of NW Electronic Properties. In general, FETs can be constructed into two distinct operation modes, namely depletion mode (D-mode) and enhancement mode (E-mode), and both device modes are needed for the assembly of electronic circuits. However, most of the III–V NW FETs operate in the D-mode which is unfavorable for the energy-efficient circuit design as a gate voltage is required to achieve the device OFF state. In order to control the device operation modes, we propose a facile "metal-cluster-decoration" method which allows manipulations of the threshold voltages (V_{TH}) of n-type III–V NWFETs based on the work function difference between the metal clusters deposited and the NW materials [39]. As a demonstration, 1.0 nm thick Au and 20 nm thick Al_2O_3 were sequentially deposited onto as-fabricated InAs NW FETs (where the Al_2O_3 is anticipated to behave as a protection or passivation layer), and the electrical performances of the InAs NW FET were measured both before and after the Au cluster decoration. As shown in Figure 8, the InAs NWFET operates initially in the D-mode, as the device exhibits non-zero drain current at the zero gate voltage; however, after the Au cluster decoration, the V_{TH} shifts positively and thus make the NWFET operated in the E-mode. Quantitative assessment reveals that a V_{TH} shift of ~4 V is obtained by the 1.0 nm thick Au decoration. In addition, in a control experiment, where the InAs NW FET is only decorated with 20 nm Al_2O_3, no shift of the V_{TH} is observed; instead, the Al_2O_3 layer just greatly reduced the device hysteresis. In this case, the role of Au cluster decoration is experimentally demonstrated to move positively the V_{TH} of InAs NWFETs and transform the device operation from D-mode to E-mode while the Al_2O_3 layer can protect the device from the detrimental influences of the ambient environment. Further experiments on the V_{TH} manipulation effects of different metals (including Ni, Cr, and Al) indicate that the V_{TH} has a strong dependence on the work functions of the metal clusters deposited. Basically, for the decoration with low work function metals clusters (e.g., Al), the V_{TH} is negatively shifted for the D-mode NW transistors, whereas for the high work function metal clusters (e.g., Au), the V_{TH} is positively moved and thus E-mode device operation are obtained. The same trend is also observed in NW devices with other III–V compositions, including InP and $In_{0.6}Ga_{0.4}As$. The metal cluster induced V_{TH} shifts can be understood through a band-bending model. Specifically, the prepared InAs NWs are intrinsically n-type with the Fermi level, E_F, lying near or slightly pinned above the conduction band edge at equilibrium (V_{GS} = 0 V) because of the relatively high free electron concentration induced from the NW surface defects; therefore, a negative gate bias is required to move the bands up or push the E_F down in order to deplete the free carriers to achieve the device off-state, which is known as D-mode device operation. When

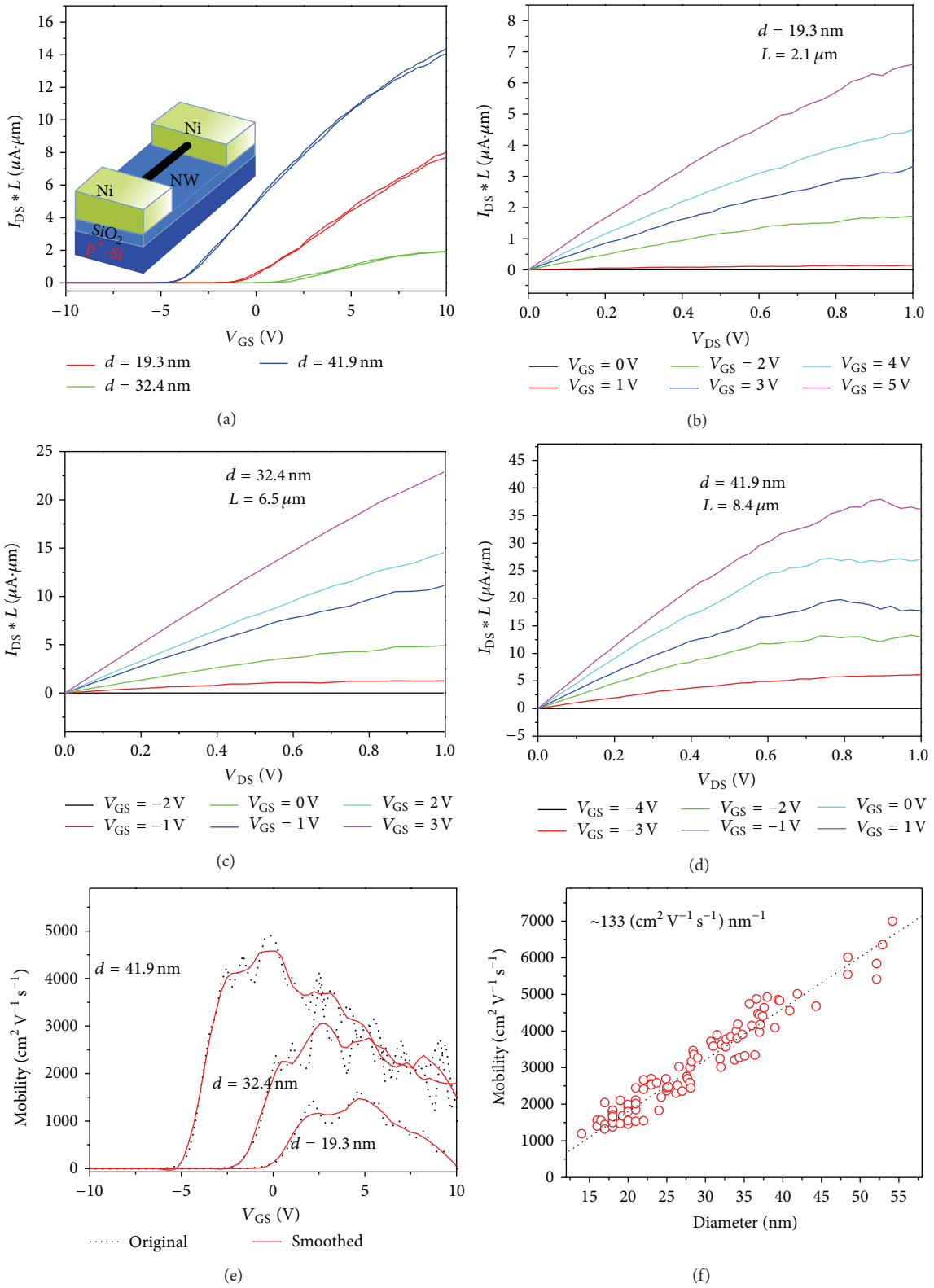

FIGURE 6: Electrical characterization of $In_{0.7}Ga_{0.3}As$ NW FETs with different NW dimensions. (a) Transfer characteristics of three back-gated $In_{0.7}Ga_{0.3}As$ NW FETs with different NW diameters (d = 19.3, 32.4, and 41.9 nm, after the native oxide deduction) for V_{DS} = 0.1 V. The inset shows the transistor schematic with Ni S/D metal contacts. (b)–(d) Output performance of the three corresponding devices as shown in (a). (e) Field-effect electron mobility assessment for the same set of NW FETs under V_{DS} = 0.1 V as presented in (a). The black dotted line is the experiment data while the solid red line is the smoothed data curve. (f) Peak field-effect mobility as a function of NW diameter for ~100 NWs with the diameters ranging from 14 to 54 nm. Reproduced from [37] with permission from The American Institute of Physics.

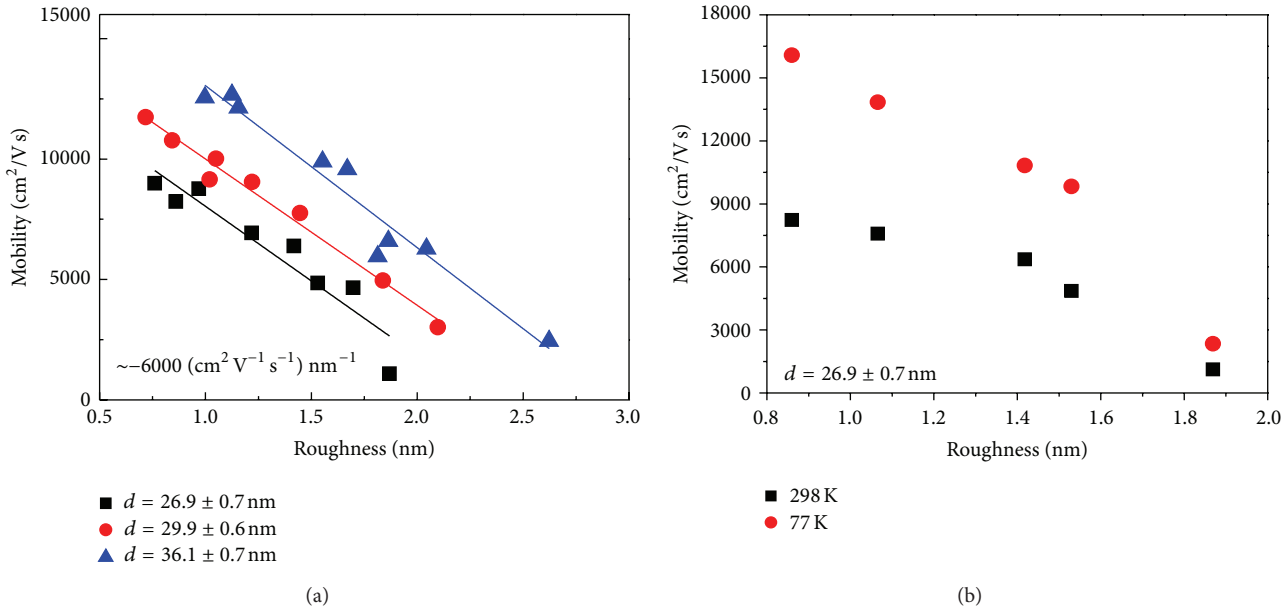

FIGURE 7: (a) Peak field-effect mobility as a function of surface roughness for NWs with three different diameter ranges: 26.9 ± 0.7 nm, 29.9 ± 0.6 and 36.1 ± 0.7 nm. Over this NW roughness range, the mobility decreases linearly with the roughness, closely fitting the linear expression with a slope of around ~ −6000 cm^2 V^{-1} s^{-1} nm^{-1}. (b) The dependency of peak field-effect mobility on the NW surface roughness (d = 26.9 ± 0.7 nm) at temperatures of 77 and 298 K. Reproduced from [38] with permission from The Institute of Physics.

the Au clusters are decorated onto the NW channel, due to the large positive work function difference ($W_M - W_S$), the equilibrium band structure is locally disturbed to induce a upward band-bending at the Au/NW interface such that the free electrons are depleted to move the E_F down to the intrinsic level, E_i (V_{GS} = 0 V), causing a positive shift in the device V_{TH}. As such, the NW device would exhibit a zero current at the off-state at a zero gate bias unless a positive gate bias is applied to push the bands down to extract the carriers (E-mode characteristics). On the contrary, when Al clusters are deposited, the negative $W_M - W_S$ would create a downward band-bending at the Al/NW interface so that free electrons are donated to the NWs leading to a higher on-current and a negative shift in the device V_{TH}. With this simple method, both D-mode and E-mode devices can be obtained, which provides broad opportunities for energy-efficient circuit applications.

4. Device Applications of III–V NWs

Having discussed the synthesis and property manipulation of III–V NWs, here, we illustrate a few examples to demonstrate their potential applications. It is known that for bulk metal-semiconductor contacts, metal-induced gap states often determine the Schottky barrier heights rather than the work function of metals used as a result of Fermi level pinning by the interface states [59]. On the other hand, NWs synthesized via VLS or VSS typically have catalytic clusters at the NW tips where the nanoscale contact between the metallic catalyst and the semiconductor should be extremely conformable with minimized interfacial states. In this regard, this nanoscale contact can be utilized to realize NW photovoltaic devices by forming additional high-quality Schottky junctions at the other end of NWs [40]. For example, Figure 9(a) presents the Au-catalyzed GaAs NWs grown with the catalytic tips (Au-Ga alloy) confirmed by SEM. It is clear that the typical tipped device exhibits a gigantic resistance in the dark due to the low intrinsic carrier concentration of the NW as well as the improper electrical contacts of the devices. However, upon illumination, the device exhibits obvious photovoltaic behavior which delivers a V_{oc} of ~0.6 V, a J_{sc} of ~11 mA/cm^2, and a fill factor (FF) of ~0.42, corresponding to an overall energy conversion efficiency of ~2.8% under AM 1.5 G illumination (100 mW/cm^2). For comparison, similar asymmetric Ni/NW/Au device with bare NWs (in which the catalyst tips are removed by sonication) and thermal evaporated electrodes exhibits a much smaller V_{oc}, J_{sc}, and efficiency (Figure 9(b)) due to Fermi level pinning of the GaAs NWs at both contacts, which emphasizes the effective formation of Schottky barrier at the catalytic tip/nanowire contact interface. This study may provide a novel configuration for NW photovoltaics, and the resulting efficiency might be further improved by minimizing the inactive GaAs NW channel.

The most intriguing property of III–V NWs lies in their achievable ultrahigh carrier mobilities, making them highly attractive materials for next generation electronic devices. Especially, recent advances of NW contact printing technology have provided a useful platform for NW assembly and integration [9–14]. Combining the contact printing approach with our "Metal-Cluster-Decoration" method, we can obtain both depletion mode (D-mode) and enhancement mode (E-mode) FETs with parallel NW arrays at well-defined locations. Based on that, n-channel metal oxide-semiconductor

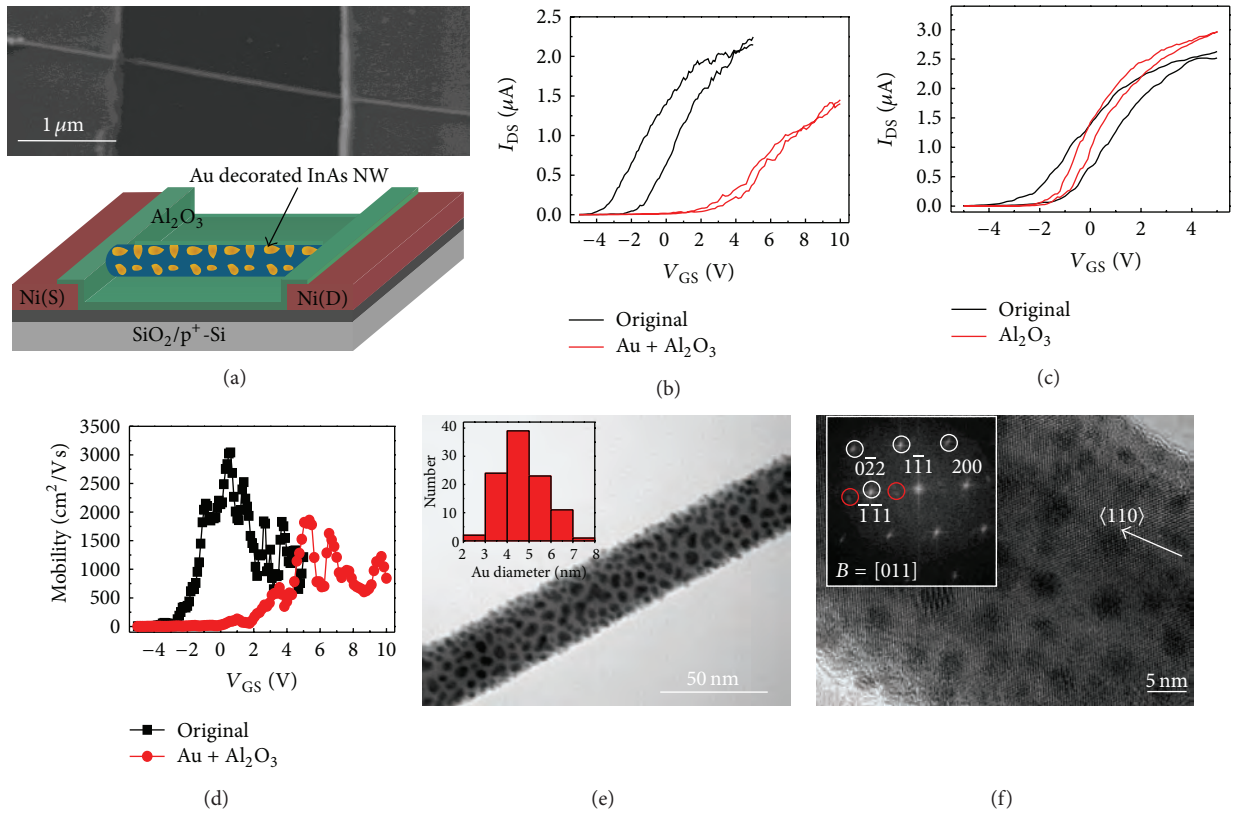

FIGURE 8: Au cluster decoration on InAs NWFETs. (a) Typical SEM image and schematic configuration of an Au decorated InAs NWFET. (b) I_{DS}-V_{GS} curves of the InAs NWFET before and after the decoration (decoration: Au cluster with an equivalent film thickness of 1.0 nm covered with a 20 nm thick evaporated Al_2O_3 layer; V_{DS} = 0.1 V). (c) I_{DS}-V_{GS} curves of the InAs NWFET before and after Al_2O_3 deposition (control; V_{DS} = 0.1 V). (d) Field-effect electron mobility of the InAs NWFET as a function of gate voltage before and after the Au cluster decoration (V_{DS} = 0.1 V). (e) TEM image of the InAs NW after the decoration and inset is the diameter distribution statistic of decorated Au clusters. (f) HRTEM image of the Au cluster decorated InAs NW and inset is the corresponding FFT. Reproduced from [39]. with permission from WILEY-VCH Verlag GmbH and Co. KGaA.

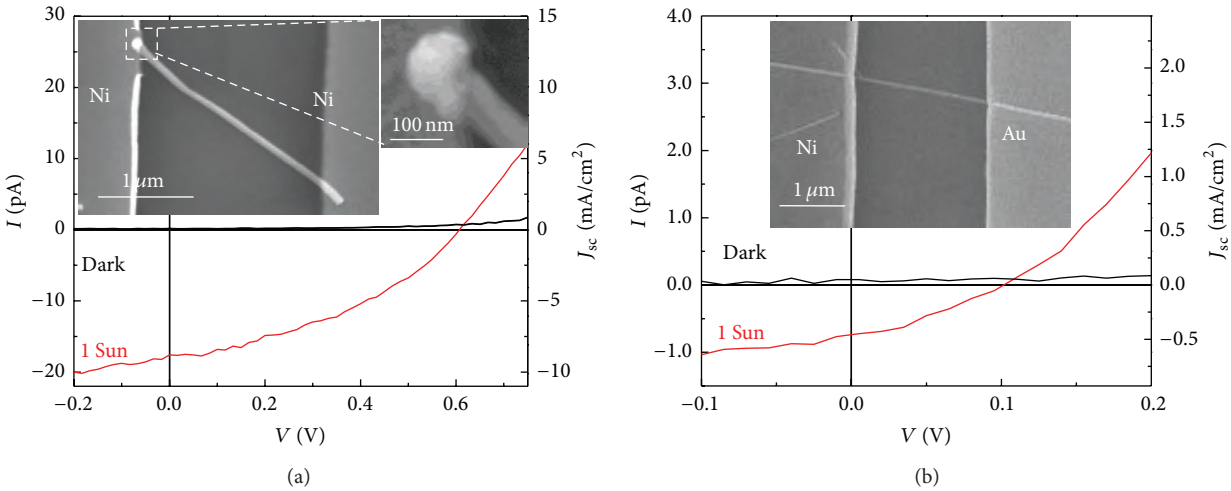

FIGURE 9: Typical I-V curves of the single GaAs NW photovoltaic device under the dark and 1 sun illumination (AM1.5 G, 100 mW/cm^2) with the current density (J) normalized to the light absorption cross-sectional area (right axis). Insets show the corresponding SEM images of the devices. (a) The NW diameter is ~70 nm with the Au-Ga alloy tip and Ni as electrical contacts and (b) the NW diameter is ~60 nm contacted with Au and Ni electrodes without any catalytic tip involved. Reproduced from [40] with permission from The American Institute of Physics.

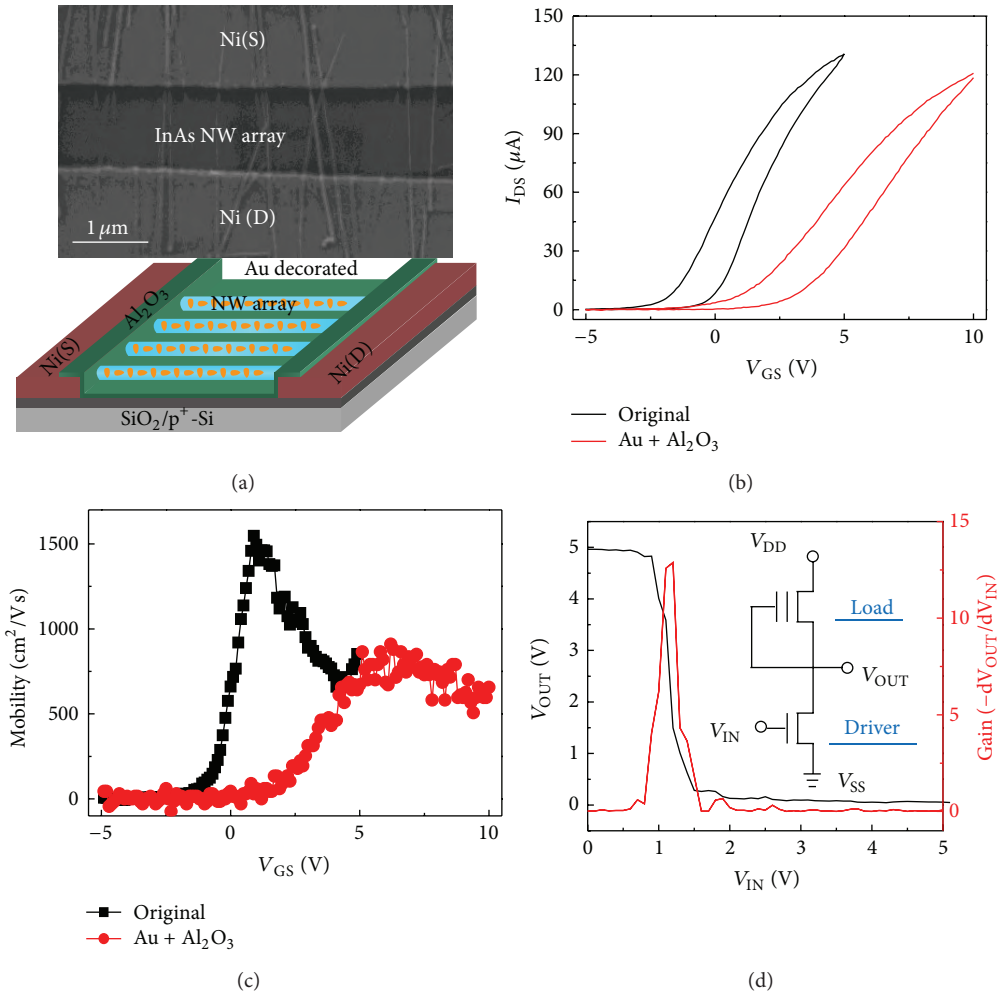

FIGURE 10: Application of the metal decoration method in transforming printed NW parallel array devices into E-mode and in the fabrication of NMOS inverters composed of an E-mode and D-mode NWFETs. (a) SEM image and schematic illustration of an Au-cluster-decorated InAs NW array FET. (b) I_{DS}-V_{GS} curves before and after decoration (decoration: Au clusters with an equivalent film thickness of 1.0 nm covered with a 20 nm thick evaporated Al_2O_3 layer; V_{DS} = 0.1 V). (c) Field-effect mobility of an InAs NW array FET before and after decoration (V_{DS} = 0.1 V). (d) The voltage transfer characteristics (red) and the corresponding gain (black) of the representative NMOS inverter, the inset is the schematic circuit diagram of the inverter. Reproduced from [39] with permission from WILEY-VCH Verlag GmbH and Co. KGaA.

(NMOS) inverters are constructed, with Au-decorated E-mode InAs NW FETs as the drivers and original D-mode InAs NW FET as the loads. Figure 10 shows the device structure of NW array FETs and the electrical characteristics of FETs as well as the NMOS inverters [39]. The transfer curve in Figure 10(d) demonstrates clearly that the input signal is inverted with a high gain ($-dV_{OUT}/dV_{IN}$) of ~13. More importantly, due to the high electron mobility and low operating voltage of these InAs NWs, the power dissipation of this III–V NW NMOS inverter is found to be respectively low. Specifically, there is no power consumed at 0 V input as a result of the "OFF" state of the driver; on the other hand, at 5 V input, the output current is the saturation current of the load at 0 V gate bias (~0.8 μA). As such, the static power dissipation is estimated to be as low as ~4 μW, which is comparable to the lowest NW NMOS reported values and far lower than their planar counterparts [60, 61].

Apart from NMOS, CMOS is also needed for the complex circuit design. We have demonstrated the controllable formation of these p-type and n-type GaAs NWs obtained *via* different growth techniques such as single-step and two-step method in order to manipulate the crystal defects. In this case, integration of these NWs into CMOS inverters has been realized as well. As given in Figure 11 [33], the output voltage is clearly transformed to the inverse of the input with different V_{DD} of 2–5 V (0 V is logic "low", while 2–5 V is logic "high") and a gain (defined as $-dV_{OUT}/dV_{IN}$) of ~2.5 is achieved with the efficient response to alternating voltage at 1 Hz with V_{DD} = 2 and 5 V. All of these confirm the validation of *in-situ* transformation of the input voltage. Although there is still a margin for the inverter to enhance the gain to enable higher frequency response, it is already the first illustration of an all intrinsic unintentionally doped GaAs NW fabricated CMOS inverter, showing the successful

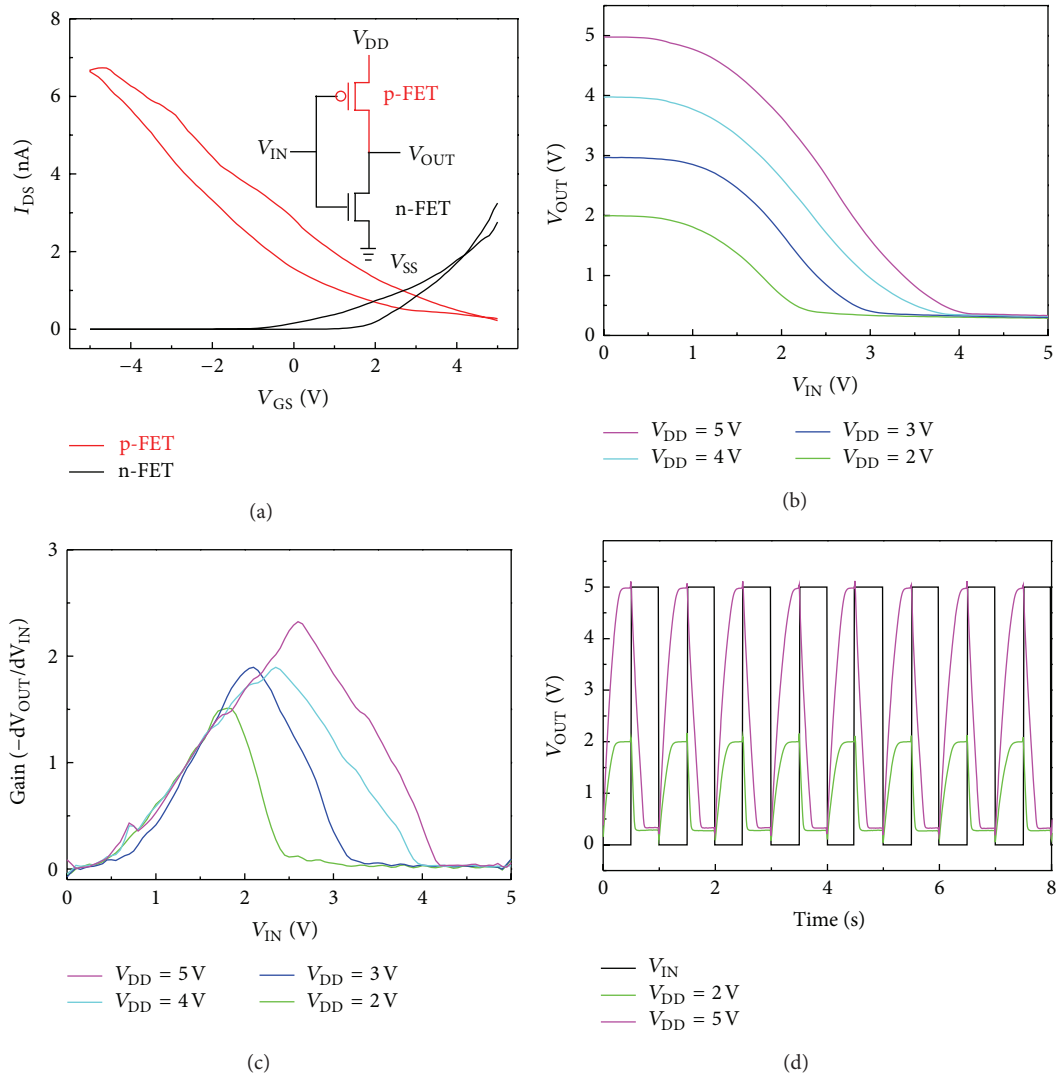

Figure 11: CMOS inverter composed of FETs with one p-type NW (two-step grown) and one n-type NW (single-step grown). (a) I_{DS}-V_{GS} curves of the corresponding p-FET and n-FET, and the inset illustrates the equivalent circuit diagram. (b) Transformation curves of the typical NW CMOS inverter. (c) Corresponding gain as a function of the input voltage. (d) Output response to the alternating voltage input of 1 Hz. Reproduced from [33] with permission from The American Chemical Society.

modulation of NW electronic transport properties by simply controlling the crystal quality, holding the promise for next-generation NW electronics by this facile management of catalytic alloy supersaturation.

5. Conclusion

In summary, semiconductor NW materials have attracted huge research attention for nearly two decades. In this review, we attempted to illustrate some recent progresses made in the area of III–V NWs, covering from the cost-effective synthesis, property manipulation to the device applications. Because of the simple setup and good controllability, the solid-source CVD approach has been widely employed for the growth of various III–V NW materials. Generally, by properly controlling the experimental parameters such as the source composition, catalyst, growth temperature, duration time and gas flow, and so forth, NWs with different chemical composition, morphology and tailorable properties could be synthesized, which provides broad opportunities for exploring the potential applications of NWs. It is worth noting that owing to the miniaturized radial dimension and large surface-to-volume ratio, NW properties are found to be influenced by many factors, including the catalyst choice, diameter, surface roughness, and so forth. Meanwhile, the external environment could also have significant effect on their properties. Understanding these factors is essentially important for the optimization of corresponding device performance; while on the other hand, these factors could be intentionally utilized in order to manipulate the NW properties. With the progresses made in the NW synthesis and assembly, many fascinating applications of NWs have

as well been demonstrated in electronics and photovoltaics. However, there still requires a substantial effort to put NW materials into practical applications, demanding more systematic investigation as well as technological innovations from their synthesis to the device design.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

[1] C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bulletin*, vol. 32, no. 2, pp. 99–108, 2007.

[2] A. I. Hochbaum and P. Yang, "Semiconductor nanowires for energy conversion," *Chemical Reviews*, vol. 110, no. 1, pp. 527–546, 2010.

[3] C. M. Lieber, "Semiconductor nanowires: a platform for nanoscience and nanotechnology," *MRS Bulletin*, vol. 36, no. 12, pp. 1052–1063, 2011.

[4] H. Ko, Z. Zhang, J. C. Ho et al., "Flexible carbon-nanofiber connectors with anisotropic adhesion properties," *Small*, vol. 6, no. 1, pp. 22–26, 2010.

[5] F.-Y. Wang, Q.-D. Yang, G. Xu et al., "Highly active and enhanced photocatalytic silicon nanowire arrays," *Nanoscale*, vol. 3, no. 8, pp. 3269–3276, 2011.

[6] H. Ko, Z. Zhang, Y.-L. Chueh et al., "Wet and dry adhesion properties of self-selective nanowire connectors," *Advanced Functional Materials*, vol. 19, no. 19, pp. 3098–3102, 2009.

[7] A. C. Ford, J. C. Ho, Y. L. Chueh et al., "Diameter-dependent electron mobility of InAs nanowires," *Nano Letters*, vol. 9, no. 1, pp. 360–365, 2009.

[8] A. C. Ford, S. Chuang, J. C. Ho, Y. Chueh, Z. Fan, and A. Javey, "Patterned p-doping of InAs nanowires by gas-phase surface diffusion of Zn," *Nano Letters*, vol. 10, no. 2, pp. 509–513, 2010.

[9] Z. Fan, J. C. Ho, T. Takahashi et al., "Toward the development of printable nanowire electronics and sensors," *Advanced Materials*, vol. 21, no. 37, pp. 3730–3743, 2009.

[10] T. Takahashi, K. Takei, J. C. Ho, Y. Chueh, Z. Fan, and A. Javey, "Monolayer resist for patterned contact printing of aligned nanowire arrays," *Journal of the American Chemical Society*, vol. 131, no. 6, pp. 2102–2103, 2009.

[11] A. C. Ford, J. C. Ho, Z. Fan et al., "Synthesis, contact printing, and device characterization of Ni-catalyzed, crystalline InAs nanowires," *Nano Research*, vol. 1, no. 1, pp. 32–39, 2008.

[12] T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, and A. Javey, "Parallel array InAs nanowire transistors for mechanically bendable, ultrahigh frequency electronics," *ACS Nano*, vol. 4, no. 10, pp. 5855–5860, 2010.

[13] Y.-Z. Long, M. Yu, B. Sun et al., "Recent advances in large-scale assembly of semiconducting inorganic nanowires and nanofibers for electronics, sensors and photovoltaics," *Chemical Society Reviews*, vol. 41, no. 12, pp. 4560–4580, 2012.

[14] X. Liu, Y.-Z. Long, L. Liao, X. Duan, and Z. Fan, "Large-scale integration of semiconductor nanowires for high-performance flexible electronics," *ACS Nano*, vol. 6, no. 3, pp. 1888–1900, 2012.

[15] K. Tomioka, M. Yoshimura, and T. Fukui, "A III-V nanowire channel on silicon for high-performance vertical transistors," *Nature*, vol. 488, pp. 189–192, 2012.

[16] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, and C. M. Lieber, "Growth of nanowire superlattice structures for nanoscale photonics and electronics," *Nature*, vol. 415, no. 6872, pp. 617–620, 2002.

[17] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[18] J. J. Hou, N. Han, F. Wang et al., "Synthesis and characterizations of ternary InGaAs nanowires by a two-step growth method for high-performance electronic devices," *ACS Nano*, vol. 6, no. 4, pp. 3624–3630, 2012.

[19] D. Spirkoska, A. Fontcuberta i Morral, J. Dufouleur, Q. Xie, and G. Abstreiter, "Free standing modulation doped core-shell GaAs/AlGaAs hetero-nanowires," *Physica Status Solidi-Rapid Research Letters*, vol. 5, no. 9, pp. 353–355, 2011.

[20] I. van Weperen, S. R. Plissard, E. P. A. M. Bakkers et al., "Quantized conductance in an InSb nanowire," *Nano Letters*, vol. 13, pp. 387–391, 2013.

[21] J. Wallentin, M. Ek, L. R. Wallenberg, L. Samuelson, and M. T. Borgström, "Electron trapping in InP nanowire FETs with stacking faults," *Nano Letters*, vol. 12, no. 1, pp. 151–155, 2012.

[22] P. M. Wu, N. Anttu, H. Q. Xu, L. Samuelson, and M. Pistol, "Colorful InAs nanowire arrays: from strong to weak absorption with geometrical tuning," *Nano Letters*, vol. 12, no. 4, pp. 1990–1995, 2012.

[23] A. I. Persson, M. W. Larsson, S. Stenström, B. J. Ohlsson, L. Samuelson, and L. R. Wallenberg, "Solid-phase diffusion mechanism for GaAs nanowire growth," *Nature Materials*, vol. 3, no. 10, pp. 677–681, 2004.

[24] R. Yan, D. Gargas, and P. Yang, "Nanowire photonics," *Nature Photonics*, vol. 3, no. 10, pp. 569–576, 2009.

[25] N. Han, A. T. Hui, F. Wang et al., "Crystal phase and growth orientation dependence of GaAs nanowires on NixGay seeds via vapor-solid-solid mechanism," *Applied Physics Letters*, vol. 99, no. 8, Article ID 083114, 2011.

[26] W. Lu and C. M. Lieber, "Semiconductor nanowires," *Journal of Physics D: Applied Physics*, vol. 39, no. 21, pp. R387–R406, 2006.

[27] K. A. Dick, K. Deppert, T. Mårtensson, B. Mandl, L. Samuelson, and W. Seifert, "Failure of the vapor-liquid-solid mechanism in au-assisted MOVPE growth of InAs nanowires," *Nano Letters*, vol. 5, no. 4, pp. 761–764, 2005.

[28] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, vol. 279, no. 5348, pp. 208–211, 1998.

[29] C. Colombo, D. Spirkoska, M. Frimmer, G. Abstreiter, and A. Fontcuberta I Morral, "Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy," *Physical Review B-Condensed Matter and Materials Physics*, vol. 77, no. 15, Article ID 155326, 2008.

[30] N. Han, F. Wang, A. T. Hui et al., "Facile synthesis and growth mechanism of Ni-catalyzed GaAs nanowires on non-crystalline substrates," *Nanotechnology*, vol. 22, no. 28, Article ID 285607, 2011.

[31] A. T. Hui, F. Wang, N. Han et al., "High-performance indium phosphide nanowires synthesized on amorphous substrates:

from formation mechanism to optical and electrical transport measurements," *Journal of Materials Chemistry*, vol. 22, no. 1, Article ID 10704, 2012.

[32] Z.-X. Yang, F. Wang, N. Han et al., "Crystalline GaSb nanowires synthesized on amorphous substrates: from the formation mechanism to p-channel transistor applications," *ACS Applied Materials and Interfaces*, vol. 5, no. 21, pp. 10946–10952, 2013.

[33] N. Han, J. J. Hou, F. Wang et al., "GaAs nanowires: from manipulation of defect formation to controllable electronic transport properties," *ACS Nano*, vol. 7, no. 10, pp. 9138–9146, 2013.

[34] Z. Yang, N. Han, F. Wang et al., "Carbon doping of InSb nanowires for high-performance p-channel field-effect-transistors," *Nanoscale*, vol. 5, no. 20, pp. 9671–9676, 2013.

[35] S.-Y. Chen, C.-Y. Wang, A. C. Ford et al., "Influence of catalyst choices on transport behaviors of InAs NWs for high-performance nanoscale transistors," *Physical Chemistry Chemical Physics*, vol. 15, no. 8, pp. 2654–2659, 2013.

[36] N. Han, F. Wang, J. J. Hou et al., "Controllable p-n switching behaviors of GaAs nanowires via an interface effect," *ACS Nano*, vol. 6, no. 5, pp. 4428–4433, 2012.

[37] J. J. Hou, F. Wang, N. Han et al., "Diameter dependence of electron mobility in InGaAs nanowires," *Applied Physics Letters*, vol. 102, no. 9, Article ID 093112, 2013.

[38] F. Wang, S. Yip, N. Han et al., "Surface roughness induced electron mobility degradation in InAs nanowires," *Nanotechnology*, vol. 24, no. 37, Article ID 375202, 2013.

[39] N. Han, F. Wang, J. J. Hou et al., "Tunable electronic transport properties of metal-cluster-decorated III-V nanowire transistors," *Advanced Materials*, vol. 25, no. 32, pp. 4445–4451, 2013.

[40] N. Han, F. Wang, S. Yip et al., "GaAs nanowire Schottky barrier photovoltaics utilizing Au–Ga alloy catalytic tips," *Applied Physics Letters*, vol. 101, no. 1, Article ID 013105, 2012.

[41] J. J. Hou, F. Wang, N. Han et al., "Stoichiometric effect on electrical, optical, and structural properties of composition-tunable InxGa1-xAs nanowires," *ACS Nano*, vol. 6, no. 10, pp. 9320–9325, 2012.

[42] B. M. Borg, K. A. Dick, B. Ganjipour, M. Pistol, L. Wernersson, and C. Thelander, "InAs/GaSb heterostructure nanowires for tunnel field-effect transistors," *Nano Letters*, vol. 10, no. 10, pp. 4080–4085, 2010.

[43] B. Ganjipour, H. A. Nilsson, B. Mattias Borg et al., "GaSb nanowire single-hole transistor," *Applied Physics Letters*, vol. 99, no. 26, Article ID 262104, 2011.

[44] A. W. Dey, J. Svensson, B. M. Borg et al., "Single InAs/GaSb nanowire low-power CMOS inverter," *Nano Letters*, vol. 12, no. 11, pp. 5593–5597, 2012.

[45] C. Yan, X. Li, K. Zhou et al., "Heteroepitaxial growth of GaSb nanotrees with an ultra-low reflectivity in a broad spectral range," *Nano Letters*, vol. 12, no. 4, pp. 1799–1805, 2012.

[46] W. Xu, A. Chin, L. Ye et al., "Charge transport and trap characterization in individual GaSb nanowires," *Journal of Applied Physics*, vol. 111, no. 10, Article ID 104515, 2012.

[47] S. Bandyopadhyay and J. Anderson, "Capacitive infrared photodetector for room temperature operation," *Applied Physics Letters*, vol. 102, no. 10, Article ID 103108, 2013.

[48] B. Mattias Borg and L. E. Wernersson, "Synthesis and properties of antimonide nanowires," *Nanotechnology*, vol. 24, no. 20, Article ID 202001, 2013.

[49] J. P. van der Ziel, R. D. Dupuis, R. A. Logan, and C. J. Pinzone, "Degradation of GaAs lasers grown by metalorganic chemical vapor deposition on Si substrates," *Applied Physics Letters*, vol. 51, no. 2, pp. 89–91, 1987.

[50] M. G. Mauk, S. Xu, D. J. Arent, R. P. Mertens, and G. Borghs, "Study of novel chemical surface passivation techniques on GaAs pn junction solar cells," *Applied Physics Letters*, vol. 54, no. 3, pp. 213–215, 1989.

[51] K. Adlkofer and M. Tanaka, "Stable surface coating of gallium arsenide with octadecylthiol monolayers," *Langmuir*, vol. 17, no. 14, pp. 4267–4273, 2001.

[52] F. Jabeen, S. Rubini, F. Martelli et al., "Contactless monitoring of the diameter-dependent conductivity of GaAs nanowires," *Nano Research*, vol. 3, no. 10, pp. 706–713, 2010.

[53] H. Hasegawa, K. E. Forward, and H. L. Hartnagel, "New anodic native oxide of GaAs with improved dielectric and interface properties," *Applied Physics Letters*, vol. 26, no. 10, pp. 567–569, 1975.

[54] M. Passlack, M. Hong, and J. P. Mannaerts, "Quasistatic and high frequency capacitance—voltage characterization of Ga2O3–GaAs structures fabricated by in situ molecular beam epitaxy," *Applied Physics Letters*, vol. 68, no. 8, Article ID 1099, 1995.

[55] S. Jin, M. V. Fischetti, and T. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: surface roughness scattering, dielectric screening, and band nonparabolicity," *Journal of Applied Physics*, vol. 102, no. 8, Article ID 083715, 2007.

[56] M. Lenzi, A. Gnudi, S. Reggiani, E. Gnani, M. Rudan, and G. Baccarani, "Semiclassical transport in silicon nanowire FETs including surface roughness," *Journal of Computational Electronics*, vol. 7, no. 3, pp. 355–358, 2008.

[57] A. Lherbier, M. P. Persson, Y. Niquet, F. Triozon, and S. Roche, "Quantum transport length scales in silicon-based semiconducting nanowires: surface roughness effects," *Physical Review B-Condensed Matter and Materials Physics*, vol. 77, no. 8, Article ID 085301, 2008.

[58] E. B. Ramayya, D. Vasileska, S. M. Goodnick, and I. Knezevic, "Electron transport in silicon nanowires: the role of acoustic phonon confinement and surface roughness scattering," *Journal of Applied Physics*, vol. 104, no. 6, Article ID 063711, 2008.

[59] F. Léonard and A. A. Talin, "Electrical contacts to one- and two-dimensional nanomaterials," *Nature Nanotechnology*, vol. 6, no. 12, pp. 773–783, 2011.

[60] A. Bindal and S. Hamedi-Hagh, "Static NMOS circuits for crossbar architectures using silicon nano-wire technology," *Semiconductor Science and Technology*, vol. 22, no. 2, pp. 54–64, 2007.

[61] A. Seyedi, A. A. Pavel, A. K. Sharma, and N. E. Islam, "Design and performance analysis of a nanoscaled inverter based on wrap-around-gate nanowire MOSFETs," *Micro and Nano Letters*, vol. 4, no. 1, pp. 16–21, 2009.