Monolayer Doping and Diameter-Dependent Electron Mobility Assessment of Nanowires

Alexandra C. Ford, Johnny C. Ho, Yu-Lun Chueh, and Ali Javey

***Abstract*—Sub-5nm ultrashallow junctions in planar and non-planar semiconductors are formed by use of a molecular monolayer doping method and conventional spike annealing. ~70% of the dopants are found to be electrically active, allowing for a low sheet resistance for a given dopant areal dose, and minimal junction leakage currents (<1 μA/cm^2) are observed. This indicates the high-quality of the ultrashallow junctions formed by this monolayer doping method. In addition, temperature-dependent current-voltage (I-V) behavior of individual InAs nanowire field-effect transistors is used to study the field-effect mobility as a function of nanowire radius. The field-effect mobility is observed to decrease with decreasing radius. The low-temperature transport behavior reveals the significant impact of surface roughness scattering on mobility degradation in smaller radius nanowires. The successful demonstration of a monolayer doping technique that does not introduce defects into the substrate, combined with a better understanding of diameter-dependent electron mobility in nanowires, contributes toward the advancement of nanoscale, electronic materials.**

***Index Terms*—Monolayer doping, ultrashallow junctions (USJs), InAs nanowires, diameter-dependent electron mobility**

I. Introduction

Device scaling has been the primary driving force behind the technological advancement in the semiconductor industry over the past few decades [1], [2]. To continue this advancement both novel methods to obtain sub-5 nm ultrashallow junctions (USJs) must be developed and new materials investigated to serve as the channel material in future devices.

Manuscript received April 3, 2009. This work was supported in part by SEMATECH, NSF, Intel Corporation, MARCO-MSD Focus Center Research Program, and the Berkeley Sensor and Actuator Center. The synthesis portion of this work was supported by a LDRD from Lawrence Berkeley National Laboratory. All fabrication was performed at the UC Berkeley Microlab facility. J. C. Ho is supported by an Intel Graduate Fellowship.

A. C. Ford is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA (e-mail: lexiford@berkeley.edu).

J. C. Ho is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA (e-mail: johnnyho@eecs.berkeley.edu).

A. Javey is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, and Berkeley Sensor and Actuator Center, University of California, Berkeley, CA 94720 USA (phone: (510)-643-7263, e-mail: ajavey@eecs.berkeley.edu).

The sub-5 nm USJ depths necessary for use with sub-10 nm gate lengths to achieve efficient electrostatics and acceptable leakage currents are difficult to realize using conventional doping strategies [1], [2]. These strategies employ a combination of ion implantation and spike annealing technology. In this method, Si atoms are displaced by dopant ions, the ions are activated and moved into the desired lattice sites, and the substrate's crystal quality is restored. The ability to use this technique to achieve sub-5 nm USJs is severely limited by transient-enhanced diffusion (TED) [3]. TED refers to the creation of point defects such as Si interstitials and vacancies that go on to interact with the dopants, thereby broadening the junction profile. Other research efforts to create shallow doping profiles while minimizing TED include the use of heavier implantation dopant sources [4]-[6] combined with either flash or laser annealing techniques [7], [8]. However, the extent to which these methods can achieve good junction uniformity and reliability and can be integrated with current IC manufacturing is relatively unknown. Here we summarize recent advancements for controlled, nanoscale surface doping of semiconductors using self-assembled dopant monolayers followed by an annealing step to diffuse in the dopant atoms. TED is minimized in this approach [9]. Here sub-5nm junction depths down to ~2 nm with low sheet resistivity using the fast diffusing dopant phosphorous are demonstrated.

In addition to novel doping strategies to drive device scaling and advancement, it is imperative to explore potential new channel materials that offer higher mobilities than Si. One such material that has both high mobility and ease of near-ohmic metal contact formation is InAs [10]-[14]. Semiconductor nanowires (NWs) especially have been shown to have great potential for use in high-performance electronics because of their size, structure, and ease of assembly on a variety of substrates using low-temperature processing conditions [15]-[17]. Smaller radius NWs are highly attractive for use as the channel material in nanoscale transistors because they permit lower leakage currents and improved electrostatics. It is therefore of technological interest to investigate the mobility-diameter dependence in InAs NWs, particularly given the contradictions in the current literature regarding the effect of nanowire miniaturization on mobility [18], [19]. The current-voltage (*I-V*) behavior at different temperatures of individual InAs NWs with ohmic contacts and the field-effect mobility as a function of radius are discussed here.

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

Authorized licensed use limited to: CityU. Downloaded on March 11,2010 at 20:52:16 EST from IEEE Xplore. Restrictions apply.

II. Materials and Methods

The monolayer doping (MLD) process is shown in Figure 1. This approach relies on the self-assembled formation of a dopant-containing monolayer on the crystalline silicon surface. The dopants are then diffused into the lattice by rapid thermal annealing. Specifically, for the phosphorous-MLD (P-MLD) process, the native SiO_2 was removed from 4 in. p-type Si wafers using 1% hydrofluoric acid (HF). The P-containing monolayer was then formed on the Si surface by reacting the wafer with diethyl 1-propylphosphonate (DPP, Alfa Aesar) and mesitylene as a solvent (25:1, v/v) at 120 ^{o}C for 2.5 hrs. The details of this monolayer formation have been reported elsewhere [9], [20]. Following the monolayer formation, a ~50 nm SiO_2 cap was evaporated by e-beam. To create n^+/p USJs, spike annealing was then performed on the substrate at 900-1050 ^{o}C in an Ar ambient to diffuse in the P atoms. A rapid thermal processing tool (AG Associate, model 610) was used for the spike annealing with a ramping rate of 100 ^{o}C/s. The 4 in. Si wafer was positioned on a 6 in. pocket wafer for the spike anneal, with the temperature monitored using a pyrometer control system. After annealing, the oxide cap was removed so the junctions could be studied.

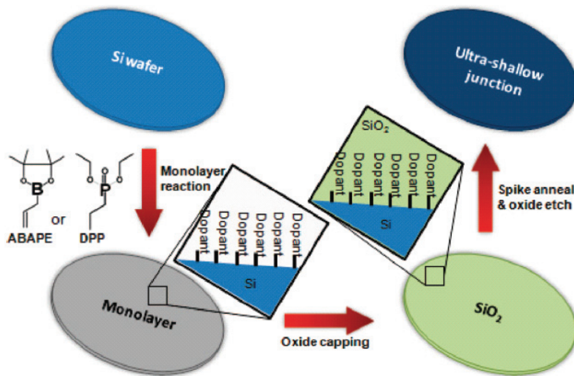

Fig. 1. Schematic showing wafer-scale monolayer doping method. (Copyright American Chemical Society, 2009 [21].)

For the portion of this work that involved the electrical characterization of individual InAs NW FETs, the growth details of the InAs NWs can be found elsewhere [22]. To summarize, the InAs wires were grown by a physical vapor transport method on SiO_2/Si substrates using Ni nanoparticles as the catalyst material. NWs grown by this method are over 10 μm long and have a radius range of 7-20 nm. The wires are untapered and have a ~2.5 nm native oxide shell. FET devices were fabricated in a back-gated geometry with source and drain patterned by photolithography and thermally-evaporated Ni as the contact material.

III. Experimental Results

Secondary ion mass spectrometry (SIMS) was used to investigate the dopant profile. Figure 2a gives the SIMS profile for P-MLD using spike anneal temperatures of 950-1050 ^{o}C.

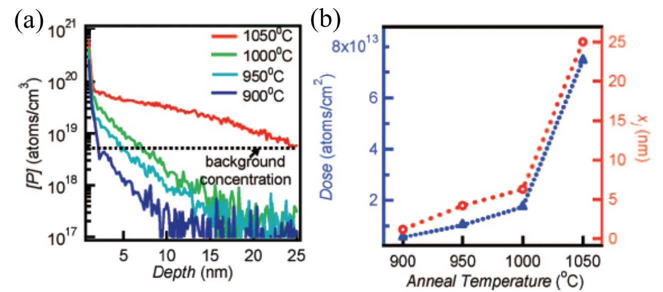

Fig. 2. Phosphorous monolayer doping characterization. (a) Secondary ion mass spectrometry (SIMS) profile of phosphorous atoms for different spike anneal temperatures. (b) Phosphorous areal dose vs. junction depth for different spike anneal temperatures. (Copyright American Chemical Society, 2009 [21].)

Around the concentration of 1-5x10^{19} atoms/cm^3 for each sample shown there is a dramatic change in the P profile, corresponding to the "kink-and-tail" characteristic. This is the result of the changeover from a vacancy-assisted mechanism to a kick-out diffusion mechanism at high and low P concentrations, respectively [23]. It is clear from this profile that the surface concentration of incorporated P increases as the annealing temperature increases. It is also evident that there is an increase in the junction depth and areal dopant dose with diffusion temperature. The junction depth x_j is the depth at which the incorporated P concentration is equal to the background B concentration of the substrate (5x10^{18} atoms/cm^3, which is the same channel doping density used in state-of-the-art Si MOSFETs). The areal dose Q is found by integration of the total area of the dopant profile. (The maximum areal dose Q depends on the monolayer packing density, which in turn depends on the "molecular footprint.") Junction depths of x_j ~2, 5, 7, 25 nm and Q ~ 5.5x10^{12}, 1.0x10^{13}, 1.7x10^{13}, and 7.5x10^{13} P atoms/cm^2 for spike anneal temperatures of 900, 950, 1000, and 1050 ^{o}C are extracted and shown in Figure 2b. Because P has enhanced diffusivity and solubility in Si at higher diffusion temperatures, this trend was anticipated. Average sheet resistance values R_s ~ 12,000, 3670, 3160, and 825 Ω/□ are observed for spike annealing temperatures of 900, 950, 1000, and 1050 ^{o}C using a noncontact sheet resistance technique. A noncontact, photovoltage measurement was used to measure average leakage currents of ~0.13, 0.55, 0.11, 0.31 μA/cm^2 for spike annealing temperatures of 900, 950, 1000, and 1050 ^{o}C. These leakage currents are close to the resolution limit of the measurement setup and provide further indication that the junctions are of high quality.

The sub-5 nm USJs with high Q facilitated by MLD clearly indicate the viability of this technology for future CMOS processing. MLD has a number of advantages over conventional ion implantation, including no TED and no removal of dopant atoms from the surface during removal of the SiO_2 cap due to the high etch selectivity of SiO_2 over crystalline Si. These results also highlight the fact that conventional annealing methods can be used to create sub-5 nm USJs.

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

Authorized licensed use limited to: CityU. Downloaded on March 11,2010 at 20:52:16 EST from IEEE Xplore. Restrictions apply.

To directly compare the n+/p USJs fabricated using the P-MLD approach to those made by other doping methods, the literature values for sheet resistance R_s and junction depth x_j for phosphorous doped junctions were compiled and are shown in Figure 3 [24]-[28].

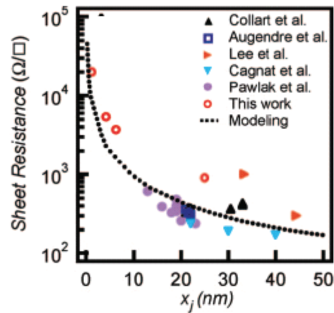

Fig. 3. Sheet resistance as a function of junction depth x_j for phosphorous doped Si using the monolayer doping method reported in this work compared to conventional doping methods found in the literature. (Copyright American Chemical Society, 2009 [21].)

For a background concentration of 5×10^{18} atoms/cm^3, the smallest x_j reported in the literature is ~13 nm with R_s ~650 Ω/cm. The lack of previously reported sub-10 nm n+/p USJs that rely on phosphorous diffusion is at least partly due to the high diffusivity of P. This further indicates the success of using the MLD approach for nanometer-scale junctions, even with fast diffusing impurities like P. In comparing junctions with x_j ~ 25 nm fabricated by the MLD method to junctions made by conventional doping techniques, it is important to note that the R_s values are comparable to within a factor of ~2. The experimental data closely fits the constant-source diffusion modeling (Figure 3), indicating the near ideal behavior of the MLD process.

Electrical properties of InAs NW FETs are illustrated in Figure 4 for NWs of radius r = 7.5-17.5 nm. Channel lengths of L = 6-10 μm were used to ensure diffusive carrier transport so that intrinsic transport properties such as carrier mobility could be extracted. While the NWs are "intrinsic" (i.e. undoped), they still exhibit n-type behavior as expected due to the high electron concentration of "intrinsic" InAs, resulting from surface fixed charges and local imbalances in stoichiometery. Ohmic metal source/drain contacts are formed to the InAs NWs as indicated by the linear dependence of the device resistance on channel length [29]. Clearly from the *I-V* characteristics, larger radius NWs exhibit larger *ON* currents and more negative threshold voltages. Length normalized *ON* currents (V_{DS} = 2V and $V_{GS} - V_t$ = 6V) of ~40, 110, and 140 μA-μm correspond to NWs of r = 7.5, 12.5, and 17.5 nm, respectively. The increase in current for larger radius wires can be attributed to larger cross-sectional area, but could also indicate a reduction in carrier scattering with increasing radius. In an effort to better understand this trend, the field-effect mobility μ_n was extracted using the *I-V* characteristics.

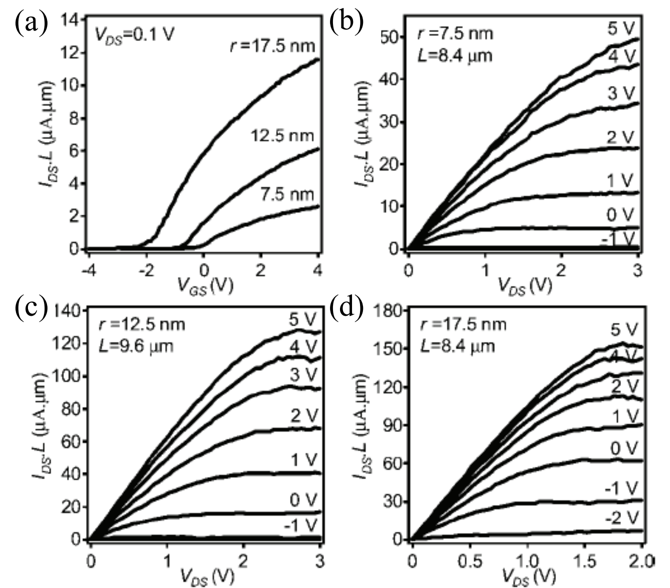

Fig. 4. *I-V* characterization of InAs NW FETs. (a) Channel length normalized $I_{DS}L$-V_{GS} plot at V_{DS} = 0.1V for three different devices with L = 8.4, 9.6, and 8.4 μm and NW radii of r = 17.5, 12.5, and 7.5 nm, respectively. Length normalized $I_{DS}L$-V_{DS} plots for different V_{GS} for the (b) 7.5 nm, (c) 12.5 nm, and (d) 17.5 nm radius NW devices. The 2.5 nm oxide shell was subtracted from the measured NW radius. NW diameters were obtained by atomic force microscopy (AFM) and scanning electron microscopy (SEM) analysis, with an uncertainty of ~ ±1 nm. All measurements were performed in vacuum with minimal hysteresis. (Copyright American Chemical Society, 2009 [30].)

Specifically, the low bias (V_{DS} = 0.1V) transconductance $g_m = (dI_{DS}/dV_{GS})|_{VDS}$ and the analytical expression $\mu_n = (g_m L^2)/(C_{ox} V_{DS})$ were used, where L is the channel length and C_{ox} is the gate oxide capacitance. Figure 5a shows the field-effect mobility as a function of V_{GS} for NWs of three different radii from the device characteristics shown in Figure 4a. The peak field-effect mobility is larger for larger radius nanowires with μ_n ~ 2500, 4000, and 6000 cm^2/(V-s) for r ~ 7.5, 12.5, and 17.5 nm.

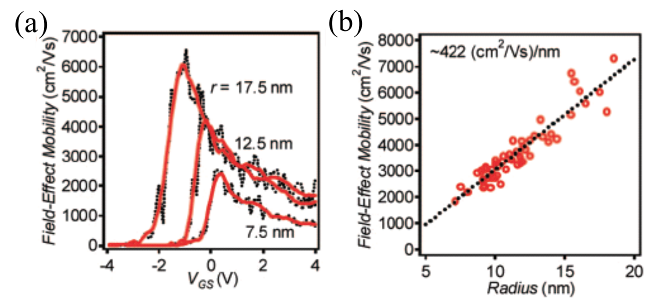

Fig. 5. Field-effect mobility assessment at room temperature. (a) Field-effect mobility vs. V_{GS} for three NWs with different radii (r = 17.5, 12.5, 7.5 nm) that correspond to the $I_{DS}L$-V_{GS} plot of Fig. 4a. (b) Peak field-effect mobility vs. radius (post oxide subtraction) for more than 50 devices. (Copyright American Chemical Society, 2009 [30].)

The sharp decay in the field-effect mobility at high electric fields can be attributed to both the increased surface scattering at high gate fields (similar to a conventional Si MOSFET) and insufficient electron injection from the metal contacts into the channel at high electric fields because of the quantization of

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

Authorized licensed use limited to: CityU. Downloaded on March 11,2010 at 20:52:16 EST from IEEE Xplore. Restrictions apply.

sub-bands (i.e. Schottky barriers to higher sub-bands may form). The InAs NWs can be taken to be a quasi-1D material because of the large Bohr radius of InAs (~34 nm) [13]. The peak field-effect mobility as a function of NW radius is shown for more than 50 different devices over a radius range of 7-18 nm. The peak field-effect mobility linearly increases with increasing radius with a slope of ~422 ($cm^2/(V\text{-}s)$)/nm. Radii outside this range could not be explored because NWs of this size could not be grown using our growth condition. The decrease in mobility with decreasing NW radius can be attributed to enhanced phonon-electron wave function overlap, increased surface scattering, increased defect scattering, and reduced gate coupling due to surface states for smaller radius NWs that have high surface area-to-volume ratio [11]. Because of the linear dependence of *ON*-state resistance with channel length, diameter-dependent contact resistance is not a factor. It can also be noted that when we extract the effective mobility (as opposed to the field-effect mobility), a similar trend of linearly increasing mobility with increasing NW radius is also observed.

To better understand the mechanisms behind the mobility degradation with decreasing NW radius, temperature-dependent electron transport measurements were performed. As expected, the peak field-effect mobility is enhanced at lower temperatures, as phonons and surface trap states are frozen out. Figure 6 shows the field-effect mobility as a function of NW radius with r = 8-20 nm for four NW FETs at 298 K and 50 K.

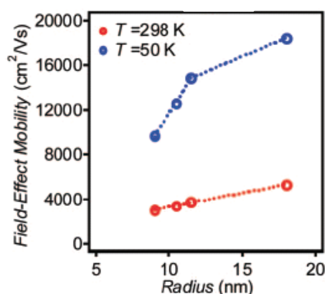

Fig. 6. Temperature-dependence of field-effect mobility vs. radius for four NWs of different radii at 298 and 50 K. (Copyright American Chemical Society, 2009 [30].)

At 50 K, the decrease in field-effect mobility with radius is even more pronounced, with a near-linear trend observed for smaller radius NWs (slope ~2077 ($cm^2/(V\text{-}s)$)/nm for $r \leq 12$ nm) and the mobility approaching a saturation value ~18,000 $cm^2/(V\text{-}s)$ for larger NWs. As most phonons and interface/surface traps are frozen out at 50 K, and impurity scattering is negligible since the InAs NWs are not intentionally doped, the dependency of field-effect mobility on NW radius can mainly be attributed to the enhanced surface roughness scattering in smaller radius NWs. With decreasing NW radius, the electron transport near the surface factors more prominently into determining the electrical characteristics. Atomic roughness at the NW surface results in increased carrier scattering which lowers the carrier mobility. Because surface roughness scattering is nearly independent of temperature, the difference in the trends observed at 298 K and 50 K in Figure 6 can be attributed to scattering by phonons, surface/interface traps, and fixed charges.

These results highlight the drastic effect of NW radius on field-effect mobility, indicating that while small radius NWs may be preferable due to their improved electrostatics and lower leakage currents, these improvements will come at the expense of mobility degradation.

IV. Conclusions

Wafer-scale formation of n^+/p USJs has been achieved through the use of self-limiting monolayer doping and conventional spike annealing. In the case of phosphorous doping, USJs in Si down to ~2 nm have been attained, with the corresponding noncontact R_s values consistent with values predicted from the dopant profiles. The extremely low junction leakage currents further indicate that the USJs formed by the MLD process are of high-quality and defect-free. This technology is also very promising for the doping of nonplanar nanoscale device structures, for example Fin-FETS or nanowire FETs.

In InAs NW FETs, the field-effect mobility increases with increasing radius for r = 7-18 nm. From low temperature transport behavior where phonons and interface traps are frozen out, the dominant effects of surface roughness scattering in smaller radius NWs are evident. This indicates that the electrostatic advantages of smaller radius nanowires are countered by the disadvantage of mobility degradation.

Acknowledgment

J. C. Ho thanks Gregory Smith, Prashant Majhi, and Joseph Bennett of SEMATECH for SIMS profiling and Jeffri Halim and Vladimir N. Faifer of Frontier Semiconductor for noncontact sheet resistance measurement.

References

[1] P. S. Peercy, "The drive to miniaturization," *Nature*, vol. 406, pp. 1023-1026, 2000.

[2] C. Claeys, "Technological challenges of advanced CMOS processing and their impact on design aspects," 17th *Int. Conf. Proc. on VLSI Design 2004*, pp. 275-282, 2004.

[3] P. A. Stolk, H. J. Grossman, D. J. Eaglesham, and J. M. Poate, "Implantation and transient boron diffusion: the role of Si self interstitials," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 96, pp. 187, 1995.

[4] Y. Kawasaki, T. Kuroi, T. Yamashita, K. Horita, T. Hayashi, M. Ishibashi, M. Togawa, Y. Ohno, M. Yoneda, T. Horshy, D. Jacobson, and W. Krull, "Ultrashallow junction formation by $B_{18}H_{22}$ ion implantation," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 237, pp. 25-29, 2005.

[5] R. MacCrimmon, J. Hautala, M. Gwinn, and S. Sherman, "Gas cluster ion beam infusion processing of semiconductors," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 242, pp. 427-430, 2006.

[6] G. H. Yon, G. H. Buh, T. Park, S. J. Hong, Y. G. Shin, U. Chung, and J. T. Moon, "Ultrashallow junction formation using plasma doping and laser annealing for sub-65 nm technology nodes," *Jpn. J. Appl. Phys.*, vol. 45, pp. 2961-2964, 2006.

Authorized licensed use limited to: CityU. Downloaded on March 11,2010 at 20:52:16 EST from IEEE Xplore. Restrictions apply.

[7] T. Ito, T. Iinuma, A. Murakoshi, H. Akutsu, K. Suguro, T. Arikado, K. Okumura, M. Yoshioka, T. Owada, Y. Imaoka, H. Murayama, and T. Kusuda, "10-15 nm ultrashallow junction formation by flash-lamp annealing," *Jpn. J. Appl. Phys.*, vol. 41, pp. 2394-98, 2002.

[8] C. H. Poon, B. J. Cho, Y. F. Lu, M. Bhat, and A. See. "Multiple-pulse laser annealing of pre-amorphized silicon for ultrashallow boron junction formation," *J. Vac. Sci. Tech. B*, vol. 21, pp. 706-709, 2003.

[9] J. C. Ho, R. Yerushalmi, Z. A. Jacobson, Z. Fan, R. L. Alley, and A. Javey, "Controlled nanoscale doping of semiconductors via molecular monolayers," *Nature Mater.*, vol. 7, pp. 62-67, 2008.

[10] X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, and C. M. Lieber, "InAs/InP radial nanowire heterostructures as high electron mobility devices," *Nano Lett.*, vol. 7, pp. 3214-3218, 2007.

[11] S. Dayeh, S. Soci, P. Yu, E. Yu, and D. Wang, "Influence of surface states on the extraction of transport parameters from InAs nanowire field-effect transistors," *Appl. Phys. Lett.*, vol. 90, pp. 162112-1-3, 2007.

[12] Q. Hang, F. Wang, P. D. Carpenter, D. Zemlyanov, D. Zakharov, E. A. Stach, W. E. Buhro, and D. B. Janes, "Role of molecular surface passivation in electrical transport properties of InAs nanowires," *Nano Lett*. vol. 8, pp. 49-55, 2008.

[13] E. Lind, A. I. Persson, L. Samuelson, and L. E. Wernersson, "Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor," *Nano Lett.*, vol. 6, pp. 1842-1846, 2006.

[14] A. C. Bleszynski, F. A. Zwanenburg, R. M. Westervelt, A. L. Roest, E. P. Bakkers, and L. P. Kouwenhoven, "Scanned probe imaging of quantum dots inside InAs nanowires," *Nano Lett.*, vol. 7, pp. 2559-2562, 2007.

[15] C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bull*. vol. 32, pp. 99-104, 2007.

[16] A. Javey, "The 2008 Kavli prize in nanoscience: carbon nanotubes," *ACS Nano*, vol. 2, pp. 1329-1335, 2008.

[17] Z. Fan, J. C. Ho, Z. A. Jacobson, H. Razavi, and A. Javey, "Large-scale, heterogeneous integration of nanowire arrays for image sensor circuitry," *Proc. Natl. Acad. Sci. USA*, vol. 105, pp. 11066-11070, 2008.

[18] S. M. Koo, A. Fujiwara, J. P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High inversion current in silicon nanowire field effect transistors," *Nano Lett*. vol. 4, pp. 2197-2201, 2004.

[19] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, and T. Hiramoto, *Symp. VLSI Tech.*, pp. 32-33, 2008.

[20] R. Yerushalmi, J. C. Ho, Z. Fan, and A. Javey, "Phosphine oxide monolayers on SiO_2 surfaces," *Angew. Chem., Int. Ed.*, vol. 47, pp. 4440-4442, 2008.

[21] J. C. Ho, R. Yerushalmi, G. Smith, P. Majhi, J. Bennett, J. Halim, V. N. Faifer, and A. Javey, "Wafer-scale, sub-5 nm junction formation by monolayer doping and conventional spike annealing," *Nano Lett.*, vol. 9, pp. 725-730, 2009.

[22] A. C. Ford, J. C. Ho, Z. Fan, O. Ergen, V. Altoe, S. Aloni, H. Razavi, and A. Javey, "Synthesis, contact printing, and device characterization of Ni-catalyzed, crystalline InAs nanowires," *Nano Res.*, vol. 1, pp. 32-39, 2008.

[23] M. Uematsu, "Simulation of boron, phosphorous, and arsenic diffusion in silicon based on an integrated diffusion model, and the anomalous phosphorous diffusion mechanism," *J. Appl. Phys.*, vol. 82, pp. 2229, 1997.

[24] E. J. H. Collarta, S. B. Felch, B. J. Pawlak, P. P. Absil, S. Severi, T. Janssens, W. Vandervorst, "Co-implantation with conventional spike anneal solutions for 45 nm n-type metal-oxide-semiconductor ultrashallow junction formation" *J. Vac. Sci. Technol. B*, vol. 24, pp. 507-509, 2006.

[25] E. Augendre, B. J. Pawlak, S. Kubicek, T. Hoffmann, T. Chiarella, C. Kerner, S. Severi, A. Falepin, J. Ramos, A. De Keersgieter, P. Eyben, D. Vanhaeren, W. Vandervorst, M. Jurczak, P. Absil, and S. Biesemans, "Superior n- and p-MOSFET scalability using carbon co-implantation and spike annealing," *Solid-State Electronics*, vol. 51, pp. 1432-1436, 2007.

[26] S. W. Yee, J. Y. Jeong, C. S. Park, J. H. Kim, J. Y. Ji, J. Y. Choi, Y. J. Lee, S. H. Han, K. M. Kim, W. J. Lee, S. K. Rha, and J. K. Oh, "The study of plasma doping process for ultrashallow junctions," *Ext. Abs. of the 7th IWJT, IEEE*, pp. 67-68, 2007.

[27] N. Cagnat, C. Laviron, D. Mathiot, C. Rando, and M. Juhel, "Shallow junction engineering by phosphorous and carbon co-implantation: optimization of carbon dose and energy," *Mater. Res. Soc. Symp. Proc.*, vol. 994, pp. 0994-F08-04, 2007.

[28] B. J. Pawlak, R. Duffy, E. Augendre, S. Severi, T. Janssens, P. Absil, W. Vandervorst, E. Collart, S. Felch, R. Schreutelkamp, and N. Cowern, "The carbon co-implant with spike RTA solution for phosphorous extension," *Mater. Res. Soc. Symp. Proc.*, vol. 912, pp. 0912-C01-06, 2006.

[29] Y. L. Chueh, A. C. Ford, J. C. Ho, Z. A. Jacobson, Z. Fan, C. Y. Chen, L. J. Chou, and A. Javey, "Formation and characterization of Ni_xInAs/InAs nanowire heterostructures by solid source reaction," *Nano Lett.*, vol. 8, pp. 4528-4533, 2008.

[30] A. C. Ford, J. C. Ho, Y. L. Chueh, Y. C. Tseng, Z. Fan, J. Guo, J. Bokor, and A. Javey, "Diameter-dependent electron mobility of InAs nanowires," *Nano Lett.*, vol. 9, pp. 360-365, 2009.

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

Authorized licensed use limited to: CityU. Downloaded on March 11,2010 at 20:52:16 EST from IEEE Xplore. Restrictions apply.